Chapter 2

2.1. The proof is as follows:

\[(x + y) \cdot (x + z) = xx + xz + xy + yz\]
\[= x + xz + xy + yz\]
\[= x(1 + z + y) + yz\]
\[= x \cdot 1 + yz\]
\[= x + yz\]

2.2. The proof is as follows:

\[(x + y) \cdot (x + \overline{y}) = xx + xy + x\overline{y} + y\overline{y}\]
\[= x + xy + x\overline{y} + 0\]
\[= x(1 + y + \overline{y})\]
\[= x \cdot 1\]
\[= x\]

2.3. Proof using Venn diagrams:

- \(x\)
- \(x + y\)
- \(y \cdot z\)
- \(x + z\)
- \(x + y \cdot z\)
- \((x + y)(x + z)\)
2.4. Proof of $15a$ using Venn diagrams:

A similar proof is constructed for $15b$.

2.5. Proof using Venn diagrams:
2.6. A possible approach for determining whether or not the expressions are valid is to try to manipulate the left and right sides of an expression into the same form, using the theorems and properties presented in section 2.5. While this may seem simple, it is an awkward approach, because it is not obvious what target form one should try to reach. A much simpler approach is to construct a truth table for each side of an expression. If the truth tables are identical, then the expression is valid. Using this approach, we can show that the answers are:

(a) Yes
(b) Yes
(c) No

2.7. Timing diagram of the waveforms that can be observed on all wires of the circuit:
2.8. Timing diagram of the waveforms that can be observed on all wires of the circuit:

\[ f = x_1 x_2 x_3 + x_1 x_2 \overline{x}_3 + x_1 x_2 x_3 + x_1 \overline{x}_2 x_3 + x_1 x_2 \overline{x}_3 + x_1 x_2 x_3 \]

2.9. Starting with the canonical sum-of-products for \( f \) get

\[ f = x_1(\overline{x}_3 + x_3) + x_2(\overline{x}_3 + x_3) + x_3(\overline{x}_1 + x_2) + x_3(\overline{x}_1 + x_3) \]

2.10. The canonical product-of-sums for \( f \) is

\[ f = (x_1 + x_2 + x_3)(x_1 + x_2 + \overline{x}_3)(x_1 + x_2 + x_3)(x_1 + \overline{x}_2 + \overline{x}_3) \cdot (x_1 + x_2 + x_3)(x_1 + \overline{x}_2 + \overline{x}_3)(x_1 + \overline{x}_2 + x_3) \]

It can be manipulated as follows:

\[ f = (x_1 + x_2 + x_3)(1 + x_2 + \overline{x}_3)(1 + \overline{x}_2 + x_3)(1 + \overline{x}_2 + \overline{x}_3) \cdot (x_2(x_1 + 1 + x_3)(x_1 + 1 + \overline{x}_3)(x_1 + \overline{x}_2 + 1) \cdot (x_2(x_1 + x_2 + 1)(x_1 + \overline{x}_2 + 1)(x_1 + x_2 + 1)(x_1 + \overline{x}_2 + 1)) \]
2.11. Derivation of the minimum sum-of-products expression:

\[ f = x_1x_3 + x_1\bar{x}_2 + \bar{x}_1x_1x_3 + \bar{x}_1\bar{x}_2x_3 \]
\[ = x_1(\bar{x}_2 + x_3) + x_1\bar{x}_2 + x_1\bar{x}_2 + \bar{x}_1 \]
\[ = x_1x_3 + (x_1 + \bar{x}_2)x_3 + (x_1 + \bar{x}_2) \]
\[ = x_1x_3 + x_2x_3 + \bar{x}_2x_3 \]

2.12. Derivation of the minimum sum-of-products expression:

\[ f = x_1\bar{x}_2\bar{x}_3 + x_1x_2x_4 + x_1\bar{x}_2x_3x_4 \]
\[ = x_1\bar{x}_2(\bar{x}_3 + x_4) + x_1x_2x_4 + x_1\bar{x}_2x_3x_4 \]
\[ = x_1\bar{x}_2x_3 + x_1\bar{x}_2(\bar{x}_3 + x_4) + x_1x_2x_4 \]
\[ = x_1\bar{x}_2x_3 + x_1\bar{x}_2 + x_1x_2x_4 \]

2.13. The simplest POS expression is derived as

\[ f = (x_1 + x_3 + x_4)(x_1 + \bar{x}_2 + x_3)(x_1 + \bar{x}_2 + x_3 + x_4) \]
\[ = (x_1 + x_3 + x_4)(x_1 + \bar{x}_2 + x_3)(x_1 + \bar{x}_2 + x_3 + x_4)(x_1 + \bar{x}_2 + x_3) \]
\[ = (x_1 + x_3 + x_4)(x_1 + \bar{x}_2 + x_3)(x_1 + \bar{x}_2 + x_4) \]
\[ = (x_1 + x_3 + x_4)(x_1 + \bar{x}_2 + x_3)(x_1 + \bar{x}_2 + x_4) \cdot 1 \]

2.14. Derivation of the minimum product-of-sums expression:

\[ f = (x_1 + x_3 + x_2)(x_1 + \bar{x}_2 + x_3)(\bar{x}_1 + \bar{x}_2 + x_3)(x_1 + x_2 + \bar{x}_3) \]
\[ = ((x_1 + x_3) + x_2)((x_1 + x_2) + \bar{x}_3)(x_1 + \bar{x}_2 + x_3) \]
\[ = (x_1 + x_2)(\bar{x}_2 + x_3) \]

2.15. (a) Location of all minterms in a 3-variable Venn diagram:
(b) For \( f = x_1 \overline{x}_2 x_3 + x_1 x_2 + \overline{x}_1 x_3 \) have:

\[
\begin{align*}
&\quad x_1 \cdot \overline{x}_2 \cdot x_3 \\
&\quad x_1 \cdot x_2 \\
&\quad \overline{x}_1 \cdot x_3
\end{align*}
\]

Therefore, \( f \) is represented as:

\[
f = x_3 + x_1 x_2
\]

2.16. The function in Figure 2.18 in Venn diagram form is:

\[
\begin{align*}
&\quad x_1 \cup x_2 \cup x_3
\end{align*}
\]

2.17. In Figure P2.1a it is possible to represent only 14 minterms. It is impossible to represent the minterms \( \overline{x}_1 x_2 x_3 x_4 \) and \( x_1 x_2 \overline{x}_3 \overline{x}_4 \).

In Figure P2.1b, it is impossible to represent the minterms \( x_1 x_2 x_3 x_4 \) and \( x_1 x_2 x_3 x_4 \).

2.18. Venn diagram for \( f = \overline{x}_1 x_2 x_3 x_4 + x_1 x_2 x_3 x_4 + \overline{x}_1 x_2 \) is
2.19. The simplest SOP implementation of the function is
\[ f = x_1 x_2 x_3 + x_1 x_2 \overline{x_3} + x_1 x_2 x_3 + x_1 x_2 x_3 \]
\[ = (x_1 + x_1) x_2 x_3 + x_1 (x_2 + x_3) \overline{x_3} \]
\[ = x_2 x_3 + x_1 \overline{x_3} \]

2.20. The simplest SOP implementation of the function is
\[ f = \overline{x_1} x_1 x_2 x_3 + x_1 x_2 x_3 + x_1 x_3 x_3 + x_1 x_2 x_3 \]
\[ = \overline{x_1} (x_1 + x_2) x_3 + x_1 (x_2 + x_3) \overline{x_3} + (x_1 + x_1) x_2 x_3 \]
\[ = \overline{x_1} x_3 + x_1 \overline{x_3} + x_2 x_3 \]

Another possibility is
\[ f = \overline{x_1} x_3 + x_1 \overline{x_3} + x_1 x_2 \]

2.21. The simplest POS implementation of the function is
\[ f = (x_1 + x_2 + x_3)(x_1 + \overline{x_2} + x_3)(\overline{x_1} + x_2 + \overline{x_3}) \]
\[ = ((x_1 + x_3) + x_1)((x_1 + x_3) + x_2)(\overline{x_1} + x_2 + \overline{x_3}) \]
\[ = (x_1 + x_3)(\overline{x_1} + x_2 + \overline{x_3}) \]

2.22. The simplest POS implementation of the function is
\[ f = (x_1 + x_2 + x_3)(x_1 + x_2 + \overline{x_3})(\overline{x_1} + x_2 + \overline{x_3})(\overline{x_1} + x_2 + \overline{x_3}) \]
\[ = ((x_1 + x_2) + x_3)((x_1 + x_2) + \overline{x_3})(\overline{x_1} + x_2 + \overline{x_3})(\overline{x_1} + x_3 + \overline{x_2}) \]
\[ = (x_1 + x_2)(\overline{x_1} + \overline{x_3}) \]

2.23. The lowest cost circuit is defined by
\[ f(x_1, x_2, x_3) = x_1 x_2 + x_1 x_3 + x_2 x_3 \]
2.24. The truth table that corresponds to the timing diagram in Figure P2.3 is

<table>
<thead>
<tr>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$x_3$</th>
<th>$f$</th>
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The simplest SOP expression is $f = \overline{x_1} x_2 x_3 + \overline{x_1} x_2 x_3 + x_1 \overline{x_2} x_3 + x_1 x_2 x_3$.

2.25. The truth table that corresponds to the timing diagram in Figure P2.4 is

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<th>$x_2$</th>
<th>$x_3$</th>
<th>$f$</th>
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The simplest SOP expression is derived as follows:

$$f = \overline{x_1} \overline{x_2} x_3 + \overline{x_1} x_2 x_3 + \overline{x_1} x_2 x_3 + x_1 \overline{x_2} x_3 + x_1 x_2 x_3$$

$$= \overline{x_1} (\overline{x_2} + x_2) x_3 + \overline{x_1} x_2 (\overline{x_3} + x_3) + (\overline{x_1} + x_1) x_2 x_3 + x_1 \overline{x_2} x_3$$

$$= \overline{x_1} \cdot 1 \cdot x_3 + \overline{x_1} x_2 \cdot 1 + 1 \cdot x_2 x_3 + x_1 \overline{x_2} x_3$$

$$= \overline{x_1} x_3 + \overline{x_1} x_2 + x_2 x_3 + x_1 \overline{x_2} x_3$$
2.26. (a) 

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<tr>
<th>$x_1$</th>
<th>$x_0$</th>
<th>$y_1$</th>
<th>$y_0$</th>
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(b) $f = (x_1 + \overline{y}_1)(\overline{x}_1 + y_1)(x_0 + \overline{y}_0)(\overline{x}_0 + y_0)$

2.27. (a) 

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<th>$x_1$</th>
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(b) The canonical SOP expression is

$$f = \overline{x}_0x_1y_1\overline{y}_0 + \overline{x}_0x_0y_0y_1 + \overline{x}_1x_0y_1\overline{y}_0 + x_1x_0y_1\overline{y}_0 + x_1\overline{x}_0y_1y_0 + x_1x_0y_1\overline{y}_0 + \overline{x}_1x_0y_1\overline{y}_0 + x_1x_0y_1\overline{y}_0 + x_1x_0y_1y_0$$
(c) The simplest SOP expression is

\[ f = x_1 x_2 + \overline{x_1} \overline{x_0} + x_1 \overline{x_0} + x_0 \overline{x_1} \]

2.30. 

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob2_30 IS
PORT ( x1, x2, x3, x4 : IN STD_LOGIC;
       f1, f2 : OUT STD_LOGIC );
END prob2_30;

ARCHITECTURE LogicFunc OF prob2_30 IS
BEGIN
  f1 <= (x1 AND NOT x3) OR (x2 AND NOT x3) OR
        NOT x3 AND NOT x4) OR (x1 AND x2) OR
        x1 AND NOT x4);
  f2 <= (x1 OR NOT x3) AND (x1 OR x2 OR NOT x4) AND
        x2 OR NOT x3 OR NOT x4);
END LogicFunc;

2.31. For the functions given in this question, it is not true that \( f_1 = f_2 \). The function \( f_1 \) is given in the form (SOP-term) AND (SOP-term). If these same two SOP terms are used for the different function \( f_1 = (SOP-term) OR (SOP-term) \) then for this new \( f_1 \) it is true that \( f_1 = f_2 \). Complete VHDL code using this new function \( f_1 \) is shown below.

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob2_31 IS
PORT ( x1, x2, x3, x4 : IN STD_LOGIC;
       f1, f2 : OUT STD_LOGIC );
END prob2_31;

ARCHITECTURE LogicFunc OF prob2_31 IS
BEGIN
  f1 <= ((x1 AND x3) OR (NOT x1 AND NOT x3)) OR
       ((x2 AND x4) OR (NOT x2 AND NOT x4));
  f2 <= (x1 AND x2 AND NOT x3 AND NOT x4)
       OR (NOT x1 AND NOT x2 AND x3 AND x4)
       OR (x1 AND NOT x2 AND NOT x3 AND x4)
       OR (NOT x1 AND x2 AND x3 AND NOT x4);
END LogicFunc;