The Multi-Standard High-Definition Video IP **Coda7542** is the pre-configurable performance upgraded video core supporting both H.264, MPEG-4, H.263, (M)JPEG encoding and MPEG-2, H.264, VC-1, MPEG-4(DivX), RealVideo, AVS and (M)JPEG decoding. Using a unique and optimal hardware architecture Coda7542 enable to meet stringent power and clock requirements at low silicon cost.

## Support Standards & Compliance

### Encoder

<table>
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<tr>
<th>Standard</th>
<th>Standard Compliance</th>
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<tr>
<td>H.264</td>
<td>Baseline Profile @L3.1</td>
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<tr>
<td>MPEG-4</td>
<td>Simple Profile</td>
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<tr>
<td>H.263</td>
<td>Profile3(Annex J, K, T)</td>
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### Decoder

<table>
<thead>
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<td>BP/MP/HP@L4.1</td>
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<td>MPEG-4</td>
<td>SP/ASP@L5.0</td>
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<td>DivX</td>
<td>High definition profile</td>
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<td>H.263</td>
<td>P3(Annex I, J, K, T)</td>
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<td>VC-1</td>
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<td>MPEG-2</td>
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<td>RealVideo</td>
<td>v.8/9/10(RMVB)</td>
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<td>AVS</td>
<td>Jizhun Profile @L6.2</td>
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<td>Sorenson</td>
<td>Sorenson spark</td>
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<td>MJPEG</td>
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## Features

### Encoding tools

- Simultaneous multi-standard encoding
- Unrestricted motion vector
- H.264 Intra-prediction
- In-loop de-blocking filter for H.264 & H.263
- MPEG-4 AC/DC prediction
- H.263 Annex J,K and T(RS=0, ASO=0)
- Error resilience tools
  - MPEG-4 : resync. Marker & Data-partitioning with RVLC
  - H.264 : FMO & ASO
- Bit-rate control(CBR & VBR)
- Built-in pre-rotation/mirroring function to remove redundant bus-loading
  - 90xn degree rotation(n=0,1,2,3)
  - Vertical/horizontal mirroring
- Dynamic clock gating for power saving
- Linear & Tiled macro-block map for bus efficiency

### Decoding tools

- Simultaneous multi-standard decoding
- CABAC/CAVLC for H.264 MP/HP
- Global motion compensation warp point1 for MPEG-4 ASP
- Built-in de-blocking, de-ringing filter and post-rotation / mirroring for post processing
- Error resilience tools
  - MPEG-4 : resync. Marker & Data-partitioning with RVLC
  - H.264 : FMO & ASO
- DivX High Definition Profile certifiable & Full Xvid compatibility
- Fully compatible with RV8/9/10 specification
- Dynamic clock gating for power efficiency
- Linear & Tiled macro-block map for bus efficiency

### Performance

- Resolution & Frame rate:
  - Decoder : up to HD(1080p 30fps / 1080i 60fps)
  - Encoder : up to HD(720p 30fps)
- MJPEG resolution
  - Decoder 32MP/s(up to 4:4:4) @133MHz
  - Encoder 64MP/s(up to 4:2:2) @133MHz
- In half-duplex mode
  - HD decoding @133MHz, encoding @180MHz
  - D1 decoding @40MHz, encoding @70MHz
- In full-duplex mode
  - D1/SD(NTSC&PAL) enc./dec. @110MHz
- Required host processor resource to run: under 1 MIPS
Applications

- Multimedia Mobile Phone
- IP Camera / DVR
- HD camcorder
- Portable Media Player
- HDTV / PVR

Internal Block Diagram

- APB I/F
- BIT Processor
- AXI Bus I/F
- Macroblock Sequencer
- Internal Peripheral Bus
- AMBA AXI BUS
- Inter-Prediction
- Intra-Prediction
- Coefficient Buffer
- AC/DC Prediction
- Rotator (Optional)
- Deblock Filter
- Transform Quantization

FPGA demonstration board Runs at 50MHz