HIT™ Cells—High-Efficiency Crystalline Si Cells with Novel Structure

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Our unique, high-efficiency c-Si solar cell, named the HIT cell, has shown considerable potential to improve junction properties and surface passivation since it was first developed. The improved properties in efficiency and temperature dependence compared to conventional p–n diffused c-Si solar cells are featured in HIT power 21™ solar cell modules and other applications which are now on the market.

In the area of research, further improvement in the junction properties of the a-Si/c-Si heterojunction has been examined, and the highest efficiency to date of 20.1% has recently been achieved for a cell size of 101 cm². The high open circuit voltage exceeding 700 mV, due to the excellent surface passivation of the HIT structure, is responsible for this efficiency. In this paper, recent progress in HIT cells by Sanyo will be introduced. Copyright © 2000 John Wiley & Sons, Ltd.

INTRODUCTION

Solar cells are gathering increasing attention as a promising means of satisfying part of the growing need for an environmentally benign energy supply. The number of solar power generation systems is expected to continue increasing, although the total power generated by them will still be small compared to world energy needs. To enable solar cells to significantly contribute to the world’s energy resources, further cost reduction must be accomplished as soon as possible.

High-efficiency solar cells offer an alternative method of cost reduction. The more power a solar cell can generate, the fewer cells are necessary to obtain the same amount of power. High-efficiency solar cells can also reduce the total system cost as well as the amount of materials needed to fabricate them. The electrical and optical design of high-efficiency solar cells has been drastically improved over the last 15 years. Electrical improvements include the passivation of the contact and surface regions of the cell, and the control of heavily doped regions in the cell as seen in the Metal–Insulator NP junction (MINP), the Back Side Point Contact, and the Passivated Emitter Rear Locally-diffused (PERL) structure. Optically, reflection has been significantly reduced and light trapping technology has been much improved. Due to these technologies, the highest efficiency to date of 24.7% has recently been demonstrated by UNSW.

These techniques, however, tend to require many photomask processes and high-temperature cycling

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of furnace steps that result in an increase in complexity and manufacturing cost. Low-quality silicon materials such as solar grade Czochralski (CZ) Si and cast polycrystalline silicon (poly-Si) are not suitable for these processes because of the degradation caused by high-temperature cycling. Therefore, many approaches have been studied to lower the process temperature and simplify the process.\(^6\)\(^-\)\(^8\)

On the other hand, we have been focusing on the development of amorphous silicon (a-Si) based solar cell technology, which is a powerful candidate for low-cost photovoltaic applications. We have already obtained the world’s highest stabilized conversion efficiency of 9.5% (JQA confirmed) for a 1200 cm\(^2\) integrated type a-Si/a-SiGe tandem solar cell.\(^9\) For higher conversion efficiency, an a-Si/thin-film poly-Si or nanocrystalline silicon (nc-Si) tandem structure is promising. To achieve the practical use of thin-film crystalline Si solar cells, however, a low-temperature junction fabrication technique is necessary. Also, from the viewpoint of simplifying the process sequence for an a-Si/poly-Si or nc-Si tandem solar cell, the junction fabrication process should be the same as that for the a-Si solar cell. On the basis of these considerations, we studied junction fabrication techniques using PECVD, and developed a new a-Si/c-Si heterojunction structure called HIT (Heterojunction with Intrinsic Thin-layer).\(^10\)-\(^13\) This structure features a very thin intrinsic a-Si layer inserted between p-type a-Si and n-type c-Si.

Recently, this novel structure has been attracting a growing amount of attention. This is because it simultaneously enables an excellent surface passivation and a p–n junction at quite a low temperature, which makes it possible to achieve high efficiency using solar grade CZ materials.\(^13\)

In this paper, the features of the HIT structure are reviewed. Sanyo started the mass production of HIT cells in 1997. Some of the HIT cell modules on the market will be introduced. Furthermore, our recent results on efficiency with the excellent surface passivation of the HIT cell are reported.

**HIT structure**

Figure 1 shows the structure of the HIT cell, which is now being mass-produced. The thickness of the randomly textured solar grade CZ Si (~1 \(\Omega\) cm) substrate is ~250 \(\mu\)m, which is thinner than that of conventional p–n diffused solar cells. The p–n junction is realized by the deposition of non-doped a-Si and p-type a-Si layers on an n-type c-Si substrate with the PECVD method. On the bottom side, the Back Surface Field (BSF) structure is used with non-doped a-Si and n-type a-Si layers. On both doped layers, transparent conductive oxide (TCO) layers and metal electrodes are formed with the sputtering and screen printing method, respectively. All processes (including metallization process) are done at temperatures of below 200°C. The TCO layer on the top also works as an anti-reflection (AR) layer. The finger electrode on the AR layer is fabricated with 2 mm spacing, which is narrower than that of conventional p–n diffused solar cells, to compensate for the poor sheet resistance of the TCO layer, whose thickness is optimized for AR coating. As for the electrode on the back, we also use a finger electrode to make the HIT cell symmetrical so that we can reduce the thermal and mechanical stresses in the device, and make this solar cell suitable for various applications, such as the bifacial modules mentioned later. This symmetrical structure and the low temperature processes offer the advantage of decreasing the thickness of the cell.

![Figure 1. The structure of the HIT cell](image-url)
Development of the HIT cell

In the beginning of our research on the a-Si/c-Si heterojunction, we investigated p–n junction fabrication processes by depositing p-type a-Si directly onto n-type c-Si substrates. In these heterojunction solar cells, however, the open-circuit voltage (Voc) and fill factor were lower than those of conventional p–n diffused solar cells. From our analysis of dark I–V characteristics, these poor properties seemed to be caused by the recombination process throughout the depletion region where the a-Si/c-Si heterojunction existed. Moreover, the doped a-Si layer had a lot of mid-gap states that possibly increased the leakage current by the tunnelling process. It was expected that this tunnelling process can be suppressed by inserting the spacer which contains less density of trap levels. From this consideration, we inserted a non-doped a-Si layer between the p-type a-Si and n-type c-Si, and found that we could reduce the backward current density by 2 orders of magnitude (Figure 2) with this slight change in the structure. The suppression of the backward current density improves the Voc and hence the solar cell performance. We named this structure HIT, which stands for Heterojunction with Intrinsic Thin-layer, and investigated it in greater detail.

Next, we tried to apply the HIT structure to the back side of the cell to realize a BSF layer. It turned out that this structure was as successful as a BSF layer and provided a good surface passivation layer simultaneously. By using the HIT structure on both sides of the cell and a highly reflective metal as the back electrode, and by optimizing other conditions, we achieved a very high efficiency of 20.0% (JQA confirmed) for an aperture area of 1 cm² in 1994.

The most prominent features of the HIT cell can be summarized as follows.

1. Simple structure: A high efficiency can be obtained with no complicated structural techniques, such as partly heavy doping or a partial oxidation method.
2. Simple, low-temperature process: Due to the simple structure, the process is very simple and cost-effective. In addition, the process temperature is so low (<200 °C) that degradation of the minority carrier lifetime for the substrate is negligible even for low-quality Si materials.
3. Simultaneous realization of surface passivation and p–n junction: With the insertion of a very thin intrinsic a-Si layer at the a-Si/c-Si heterojunction, surface recombination is drastically suppressed. Therefore, during the junction fabrication process, good surface passivation on the c-Si surface is also realized.
4. The BSF structure can be realized with the same process: The HIT structure is also suitable for fabricating the Back Surface Field (BSF) structure. The same process with a different impurity can be used to obtain the BSF structure and good surface passivation.
5. Stability: The Staebler–Wronski effect, which is seen in a-Si based solar cells, is not seen in the HIT cell. This is probably due to the fact that the a-Si layers are very thin and contribute little to the power generation. Besides, the degradation of the carrier lifetime caused by the metastable defect
related to the boron–oxygen complex does not apply to the HIT cell, which uses phosphorous doped CZ Si.\(^{15}\)

6. Improved high-temperature performance: One disadvantage of c-Si solar cells for practical use is their poor high-temperature performance compared with a-Si solar cells. The HIT cell, which has both a-Si and c-Si, shows an improved high-temperature performance. A comparison of temperature dependence on the efficiency between the HIT cell and the conventional p–n diffused cell is shown in Figure 3. The HIT cell has better temperature dependence than the conventional p–n diffused cell. Figure 4 shows an output power comparison between the HIT cell and a conventional p–n diffused solar cell placed in a row at the same pitch, facing south. The deviation between the HIT cell and p–n diffusion cell increased with increasing the cell temperature. The HIT cell showed 8.8% higher output power under this condition. This improved temperature dependence is seen in the HIT cell modules, too.

**Good surface passivation with the HIT structure**

The suppression of the backward current seen in Figure 2 indicates that the HIT structure can effectively passivate the a-Si/c-Si heterointerface. From a comparison between the simulated internal quantum efficiency (IQE) and experimental IQE data of a solar cell that was irradiated from the back side, the surface recombination velocity at the interface between c-Si and a-Si on the back side was estimated to be less than 100 cm/s.\(^{13}\) As for the front, the interface recombination velocity is probably smaller than that of the back, although it cannot be correctly estimated by using the same method due to the strong
electrical field at the p–n heterojunction. We tried to investigate the effect of surface passivation directly with the carrier lifetime. The carrier lifetime of the HIT cell was measured with the laser-induced microwave-detected photoconductive-decay (μ-PCD) method by irradiating both microwaves and a probe light onto the wafer from the top and bottom side of the cell. The structure of the sample for this measurement was identical to the HIT cell shown in Figure 1, where no TCO or electrodes were fabricated. We did a series of measurements on more than 30 different wafer lots. From each wafer lot, we carefully chose a pair of substrates, which were packed side by side, to avoid the deviation in the bulk lifetime of c-Si wafers as much as possible. After texturing and cleaning processes were done on the same batch, one of each pair was passivated with iodine-methanol, and the other was sent to the a-Si deposition processes. Iodine termination is a common technique for measuring the carrier lifetime of c-Si wafers. The μ-PCD measurements were made with a WT-85 lifetime scanner system (SEMI-LAB). According to the standard PCD theory for a homogeneously doped, defect-free wafer with a spatially uniform bulk carrier lifetime, the relationship between the effective lifetime and the bulk lifetime is given by

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_b} + \frac{1}{\tau_s}.
\]

where \(\tau_{\text{eff}}\) is the effective lifetime (the measured lifetime), \(\tau_b\) is the bulk lifetime and \(\tau_s\) is the surface recombination lifetime component. As is clear from equation (1), the better the surface is passivated, the closer the effective carrier lifetime is to the bulk lifetime of a silicon wafer. If the surface of the wafer is not passivated well, \(\tau_{\text{eff}}\) becomes lower.

Figure 4 shows a comparison of the carrier lifetime of HIT cells with different irradiating configurations. Each lifetime data is plotted to that of the iodine-terminated c-Si substrate. The lifetime obtained by irradiating the probe light from the top always showed a higher value than that of the other, as we expected. It is also a very important result that, regardless of the direction of irradiation, the HIT cells showed a better carrier lifetime than the iodine-terminated substrates (the measurement data were higher than the dashed line, which indicates that lifetime data with different passivation methods were identical). Consequently, the HIT structure was proved to be an excellent surface passivation technology compared to the iodine solution.

According to a recent report by Kurita et al., the surface recombination velocity of iodine-terminated CZ Si (100), is better (~10 cm/s) than that obtained from oxide-passivated silicon surfaces. In their work, they compared the lifetime of commercial CZ c-Si, in which substrates have sufficient quality for ULSI chip processes, by changing the passivation method. Since we use a solar grade CZ Si wafer made

![Figure 5. Carrier lifetime estimated by the μ-PCD method with different surface passivation techniques, the HIT structure and iodine termination, irradiating both μ-wave and probe light to the sample from the top (circles) and bottom (diamonds) side of the cell. The dashed line indicates where the values estimated by each passivation technique are identical.](image-url)
from low-cost silicon material, it is not appropriate to directly compare the lifetime of the samples between the HIT structure and an oxide-passivated wafer. However, from the data we have obtained so far and the above discussion, we think that the HIT structure can achieve a better surface passivation than thermal oxidation passivation. We will continue to investigate the surface passivation at the a-Si/c-Si interface, where both hydrogen passivation and carrier separation caused by the strong electrical field can exist, and will report the results elsewhere.

Mass production of HIT cells

Since our success in fundamental research, we have focused our efforts on industrializing HIT cells with a larger size of $\sim 100$ cm$^2$ and have achieved a conversion efficiency of 17.3%. At the same time, we have also tried to save as much silicon material as possible by reducing the thickness of the c-Si wafer and, as mentioned before, have succeeded in realizing very thin ($\sim 250$ µm) HIT cells without warp.

Based on these results, Sanyo started mass producing HIT cells in October 1997. We named our new solar cell module HIT Power 21™ (Figure 6). This was the world’s first industrialization of a-Si/c-Si hybrid solar cells. Applying the high-efficiency HIT cells to a solar module resulted in the world’s highest module efficiency of 15.2% for production modules, and an electric output of 180 watts. This high output power can reduce the installation area by 20% compared to a conventional p–n diffusion...
Table I. Specifications of the solar cell modules with HIT cells

<table>
<thead>
<tr>
<th>Type</th>
<th>HIT Power 21\textsuperscript{TM}</th>
<th>HIT Power Roof\textsuperscript{TM}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of cells</td>
<td>96</td>
<td>96</td>
</tr>
<tr>
<td>Maximum output (W)</td>
<td>180</td>
<td>167</td>
</tr>
<tr>
<td>Optimum operation voltage (V)</td>
<td>50.7</td>
<td>48.5</td>
</tr>
<tr>
<td>Optimum operation current (A)</td>
<td>3.55</td>
<td>3.44</td>
</tr>
<tr>
<td>Dimensions of module (mm)</td>
<td>1320 × 895 × 35</td>
<td>1403 × 345 × 35</td>
</tr>
<tr>
<td>Weight (kg)</td>
<td>15</td>
<td>15</td>
</tr>
</tbody>
</table>

Figure 7. A 100 kW system with the HIT Power 21\textsuperscript{TM}

solar cell module. The specifications of the modules using HIT cells are shown in Table I and an example of a power generation system using HIT Power 21\textsuperscript{TM} is shown in Figure 7.

A solar cell module that is capable of replacing a roofing tile has also been produced. Figure 8 shows an example, called the HIT Power Roof\textsuperscript{TM}. Since this kind of module can be installed without a mounting stand and greatly simplifies installation, it is more cost effective than usual solar cell modules.

HIT Power Double\textsuperscript{TM}, a new solar cell module that generates power on both the front and back surfaces, is a unique application of the HIT cell which has a symmetrical structure. In this module, shown in Figure 9, solar cells are sandwiched between a cover glass on the front and a translucent material on the back. Under the same illumination condition, the rear can generate about 80% of the current compared to the front, although it has not been fully optimized. Figure 10 shows an example of HIT Power Double\textsuperscript{TM} installed on the roof of a building. As seen in the rear view of this module, the space between the solar cells are transparent enabling some light to pass through the module and illuminate surfaces on the other side. This module is particularly useful for ground installations because it can use the light reflected from the ground. Figure 11 shows a comparison of the output power for one day between HIT Power Double\textsuperscript{TM} and HIT Power 21\textsuperscript{TM}, when both modules are installed on
Figure 8. HIT Power Roof™, capable of replacing a ceramic roofing tile

Figure 9. A schematic diagram of the HIT Power Double™

cement at a 30-degree pitch, facing south. HIT Power Double™ can generate 8.1% more than HIT Power 21™. HIT Power Double™ is also suitable for roadside fences or other vertical installations.

High Voc HIT solar cell

Thanks to the excellent surface passivation and an improvement of interface treatment, we have recently obtained a very high Voc c-Si solar cell with the HIT structure. As is shown in Figure 12, a Voc of 702 mV and a total area efficiency of 20.1%, certified by JQA, have been achieved with the area of 101 cm². This is the highest value for solar cells fabricated at a temperature of less than 200°C. This high efficiency was achieved mainly by:

1. optimization of the surface treatment and high quality a-Si i-layer which can be estimated by lifetime measurement;
2. high quality doped layers that can make good contact to the TCO layers;
3. control of the texturing process to improve the uniformity of the textured surface.

Here, we have to emphasize that this high Voc was obtained by the same process as that for mass production. We can easily transfer some of these technologies to the production line. There are some papers about solar cells in which the Voc is more than 710 mV. In these works, they used planar c-
Figure 10. The rear view of HIT Power Double™ (this side) and HIT Power 21™ (the other side) module arrays. The electrode on the back side can be seen in HIT Power Double™

Si wafers to obtain a high Voc by reducing the total surface area, and hence, total surface recombination. The short circuit current and efficiency were consequently neglected. In our work, however, we used solar grade CZ c-Si with a textured substrate, and actually obtained a high Voc exceeding 700 mV and high conversion efficiency. It is quite encouraging that we can make high-efficiency c-Si solar cells with low-cost materials using simple fabrication technologies. In Figure 13, a typical IQE spectrum of the HIT cell is shown. In the short wavelength region (< 700 nm), there is a certain loss because of the absorption in p-type a-Si and TCO layers. From 700 to 1000 nm, the IQE is almost unity. Free carrier absorption in n-type a-Si and TCO layers cannot be neglected in the longer wavelength region (> 1000 nm).

Figure 11. A comparison of the output performance for one day between HIT Power 21™ and HIT Power Double™
nm). Besides, absorption related to the mid-gap state in the doped a-Si layers also must be considered. We think there is a room for higher Isc by improving a-Si layers.

CONCLUSION

In this paper, we have shown recent progress in the production and efficiency of the HIT cells and, surprisingly, that the HIT structure has a possibility to obtain better surface passivation than the oxidation technique. The mechanism of these a-Si/c-Si heterojunction properties, including temperature dependence, however is still under investigation. We think that a full understanding of the details of this structure will enable us to achieve even higher efficiency. We will continue investigating this structure and hope to produce more efficient HIT modules in order to contribute to the world’s energy resources.

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