EBM300 SPECIFICATION

COLOR DIGITAL CMOS CAMERA MODULE

Rev 1.0

E2BOX COMPANY
http://www.e2box.co.kr

INDEX

1. Feature

Color CMOS camera module with digital IO interface

8bit data , control signal and standard SCCB inteface

Direct image data addressing

Supports SXGA(Optional), VGA, QVGA, QQVGA, CIF, QCIF, QQCIF

1/4 inch optical Lens

YUV, RGB565/RGB555, Raw RGB Data supports

Automatic Image control function including:
Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)

Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), and anti-blooming.

Supply voltage : 3.3V

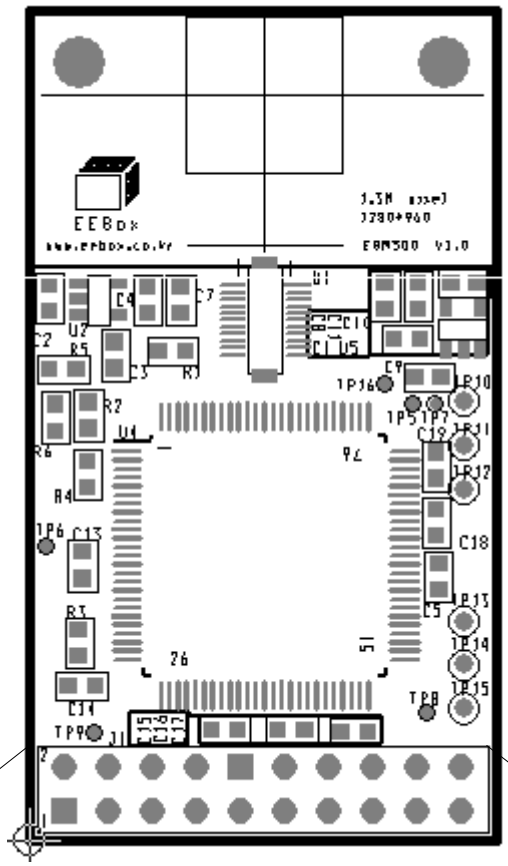
Typical Power consumption : 70mA

Maximum Power consumption : 100mA

Operation Temperature : 0℃ ~ 70℃

Dimension : 27 * 48 * 7.5 mm(Except Connector)

2. Pin Location

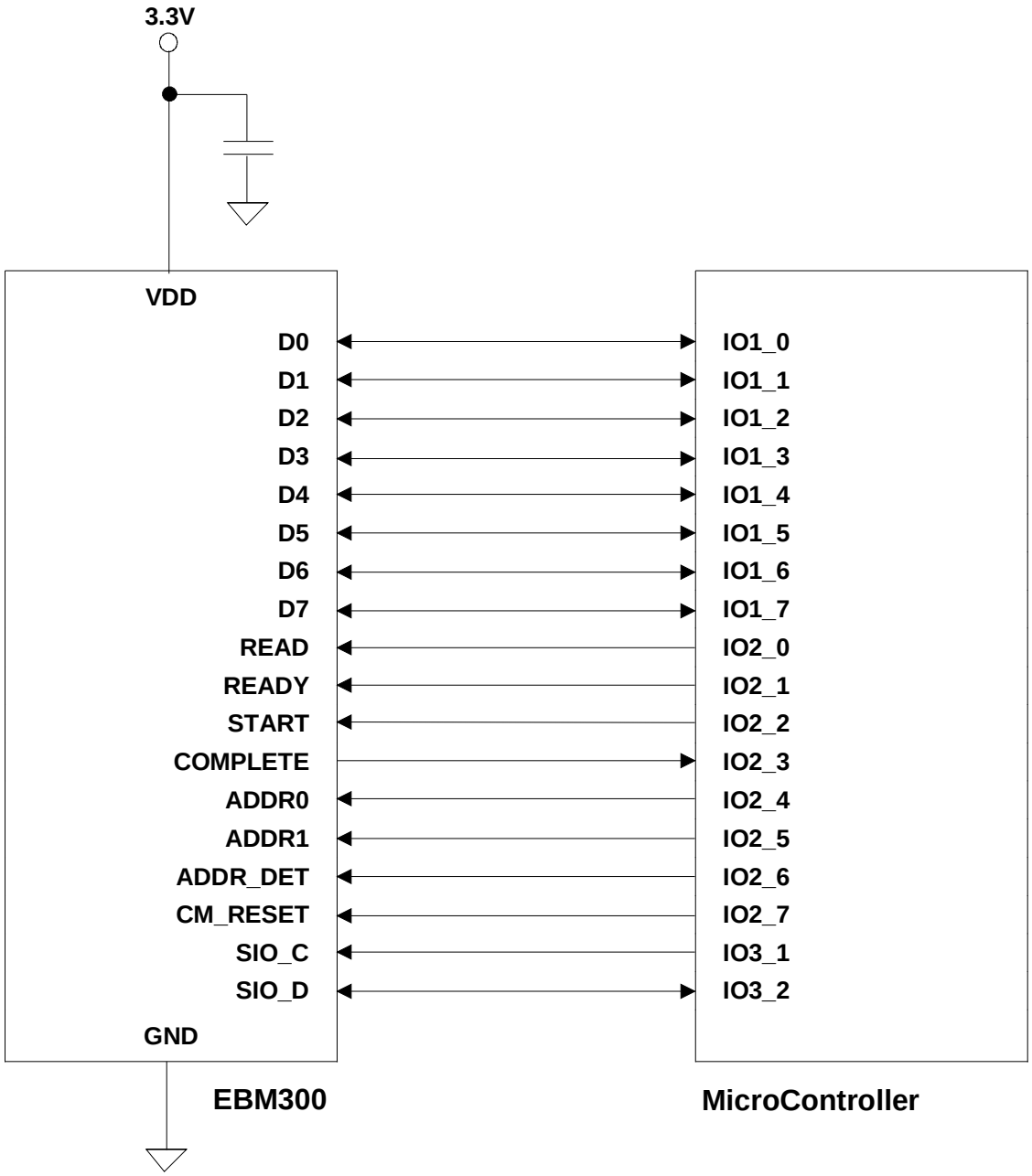


2	4	6	8	10	12	14	16	18	20
VDD	D1	D3	D5	D7	READY	COMPLETE	ADDR1	CM RESET	SIO_D
1	3	5	7	9	11	13	15	17	19
GND	D0	D2	D4	D6	READ	START	ADDR0	ADDR DET	SIO_C

3. Pin Description

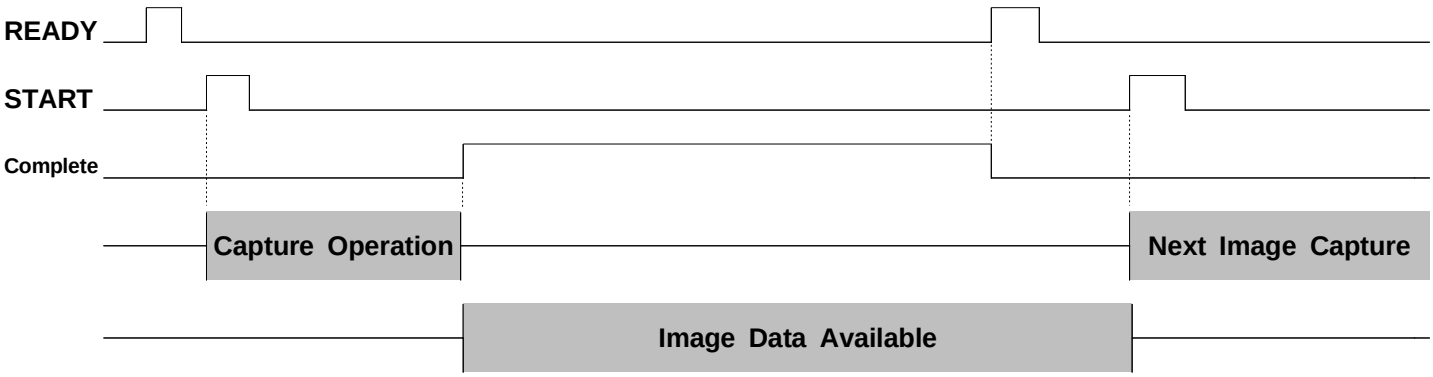
Pin	Nam	Type	Function / Description
1	GND	Power	Ground
2	VDD	Power	Power Input 3.3V
3	D0	I/O	Image data output / Address input
4	D1	I/O	Image data output / Address input
5	D2	I/O	Image data output / Address input
6	D3	I/O	Image data output / Address input
7	D4	I/O	Image data output / Address input
8	D5	I/O	Image data output / Address input
9	D6	I/O	Image data output / Address input
10	D7	I/O	Image data output / Address input
11	READ	I	Read image data. Active high (Must be asserted low when capture operation)
12	READY	I	Ready image capture. Reset address pointer. Active high. (Must be asserted low when capture operation)
13	START	I	Start image capture. Active high.
14	COMPLETE	O	Capture complete. Active high.
15	ADDR0	I	Address 0 (Must be asserted low when capture operation)
16	ADDR1	I	Address 1 (Must be asserted low when capture operation)
17	ADDR_DET	I	Address detect. Active high. (Must be asserted low when capture operation)
18	CM_RESET	I	camera reset. Clears all registers and resets them to their default values. Active high,
19	SIO_C	I	SCCB(Serial Camera Control Bus) Clock
20	SIO_D	I/O	SCCB(Serial Camera Control Bus) Data

4. Typical Applicatin

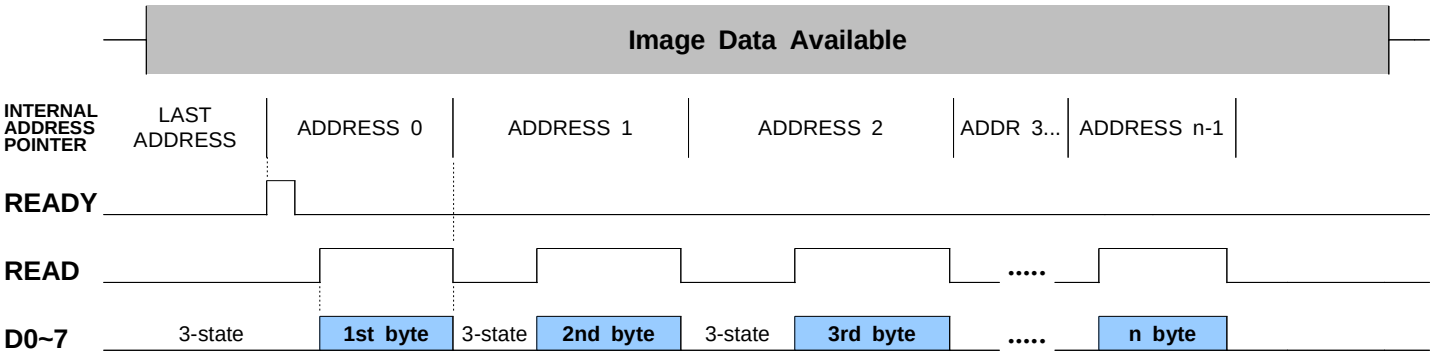


5. Image Capture

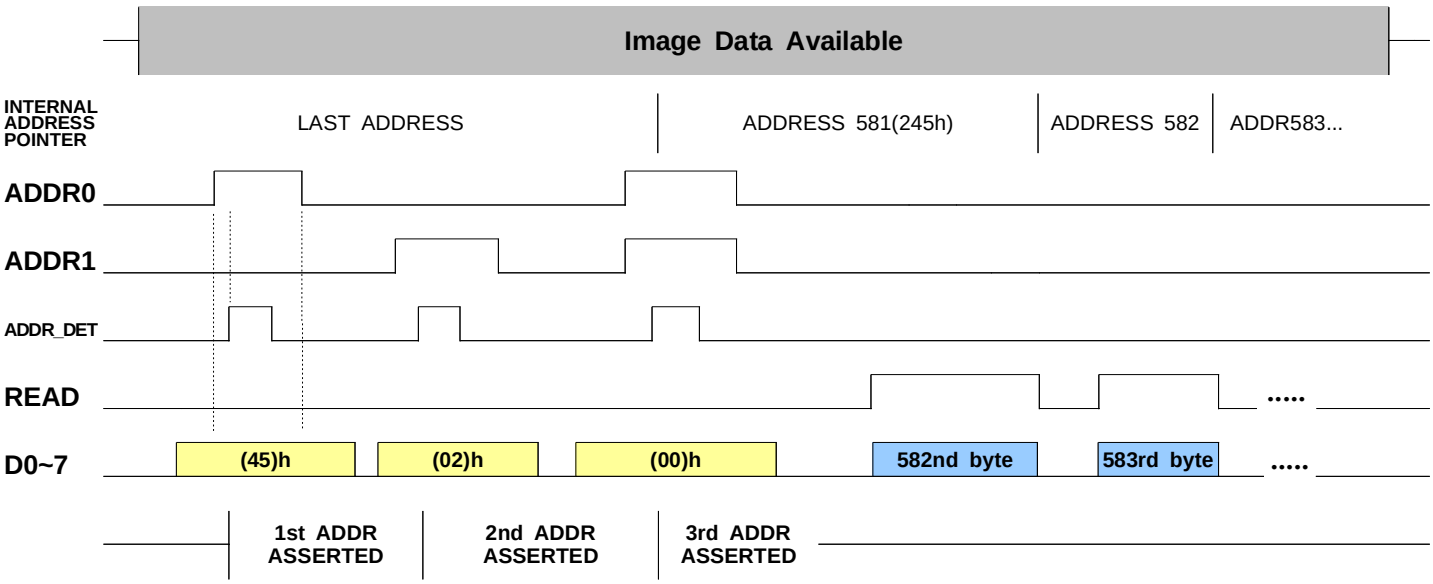
5-1. Capture Sequence



5-2. Sequential Access



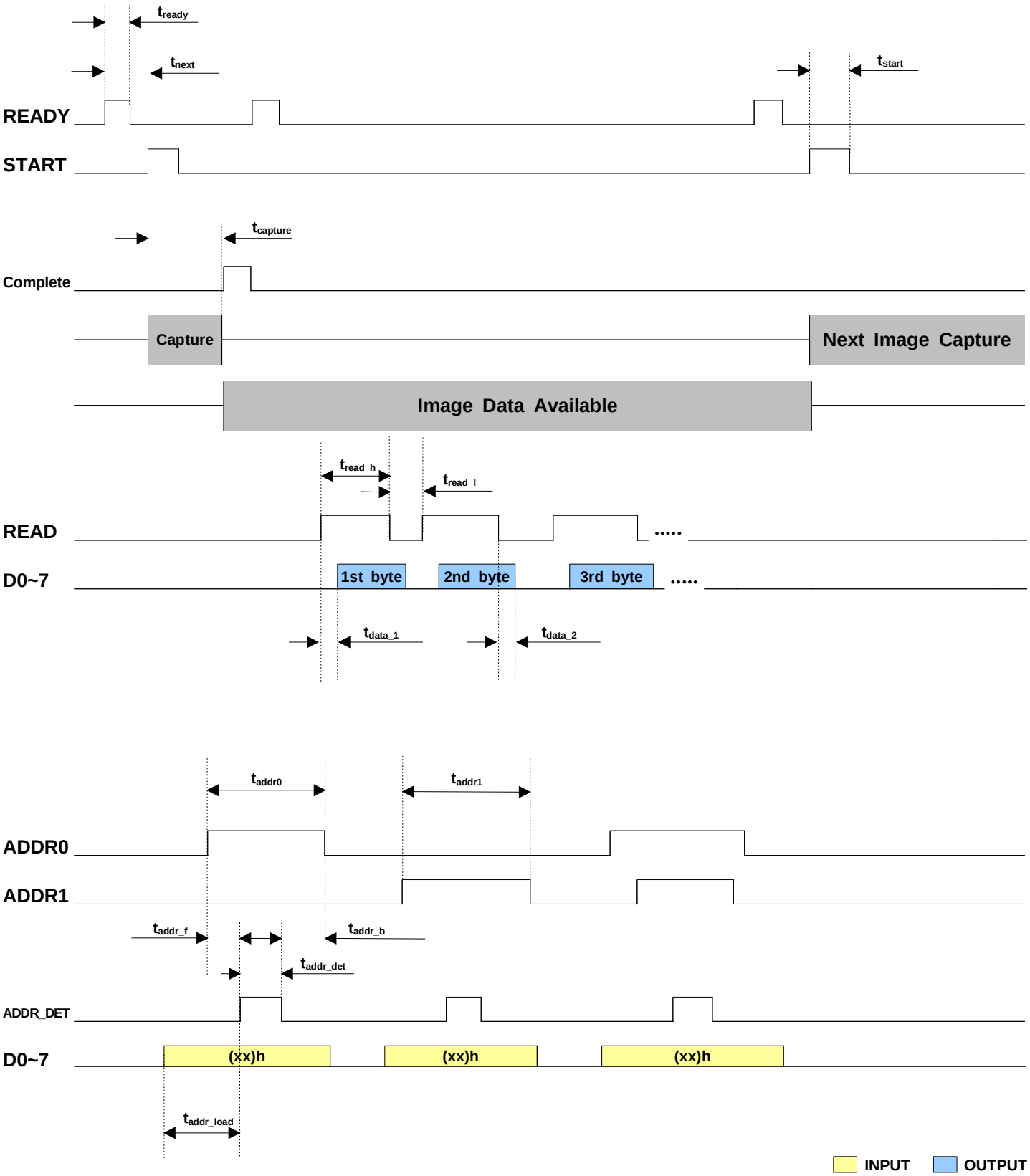
5-3. Random Access



*** ADDRESS = (cc bb aa)h , aa = 1st ADDR , bb = 2nd ADDR , cc = 3rd ADDR**

INPUT OUTPUT

6. Capture Timing



Timing Table.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{ready}	READ signal pulse width	10		ns
t_{next}	Next signal interval	10		ns
t_{start}	START signal pulse width	10		ns
$t_{capture}$	Capture operation delay time (when double clock)	n pixel*50	n pixel*100	ns
t_{read_h}	READ signal pulse width HIGH	10		ns
t_{read_l}	READ signal pulse width LOW	10		ns
t_{data_1}	Data output delay time 1		20	ns
t_{data_2}	Data output delay time 2		20	ns
t_{addr0}	ADDR0 signal pulse width	10		ns
t_{addr1}	ADDR1 signal pulse width	10		ns
t_{addr_f}	Address detection front timing	10		ns
t_{addr_b}	Address detection back timing	10		ns
t_{addr_det}	Address detection pulse width	10		ns
t_{addr_load}	Address load font timing	10		ns
t_{reset}	Reset time	5		ms

7. Absolute Maximum Ratings

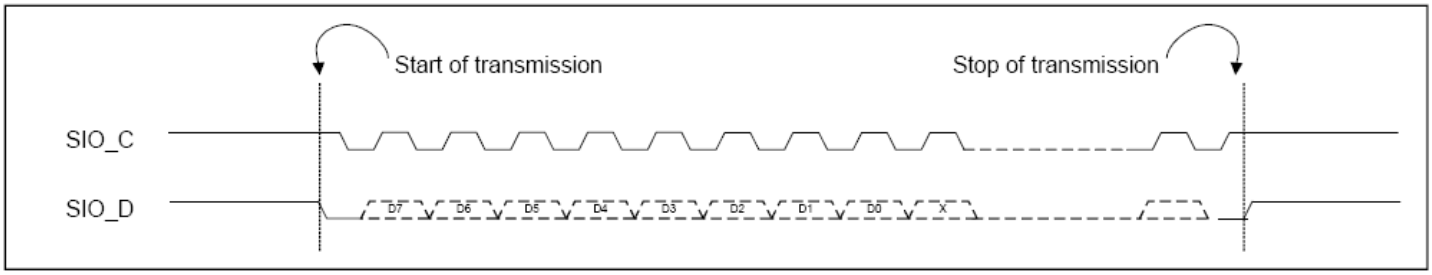
Supply Voltage : -0.3V to 3.4V
Storage Temperature : -35℃ to +120℃
Operation Temperature : 0℃ ~ 70℃

8. DC Electrical Characteristics

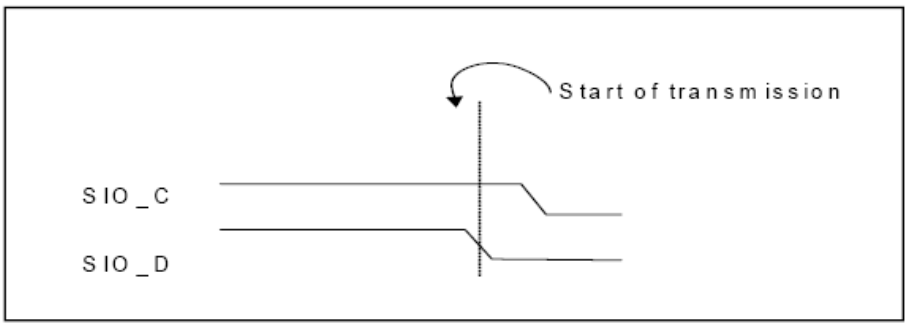
Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	3.1	3.3	3.35	V
I_{DD}	Operating Current	60	70	100	mA
V_{IH}	Input voltage HIGH	2.0		5.5	V
V_{IL}	Input voltage LOW	-0.3		0.8	V
V_{OH}	Ouput voltage HIGH	V_{DD}-0.4			V
V_{OL}	Ouput voltage LOW			0.4	V
I_{OH}	Ouput current HIGH		4		mA
I_{OL}	Output current LOW		8		mA
I_L	Input Leakage Current			15	uA

9. SCCB(Serial Camera Control Bus)

Timing Diagram of a Data Transmission

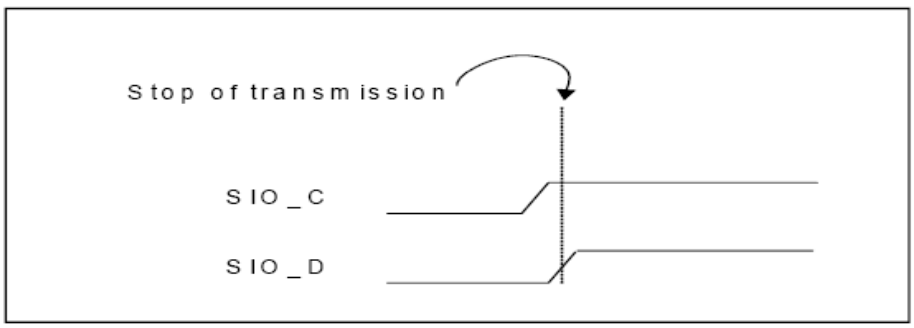


Start of Transmission



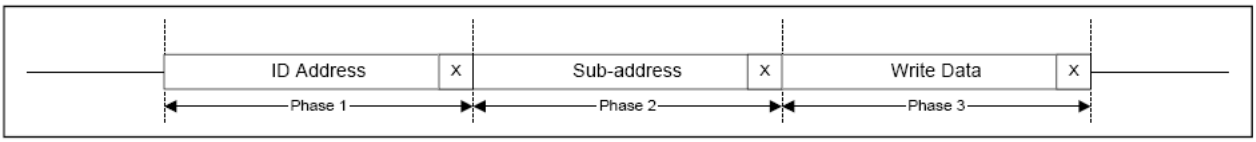
The master will drive the SIO_D signal high or "1" when the bus is idle. The start of data transmission will occur when the SIO_D is driven to low or "0" and SIO_C is high or "1".
A write or read operation will always be initiated by the master and only after the occurrence of the start condition. The write operation is completed only when the master asserts the stop condition or another start condition. Similarly, the read operation is completed only when the master asserts a stop condition or another start condition.

Stop of Transmission



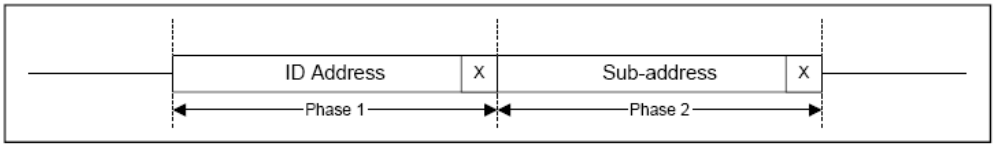
A stop of data transmission is indicated by a transition of the SIO_D signal from low or "0" to high or "1" while the SIO_C signal is high or "1".
The master will hold SIO_D high as well as maintain the SIO_C signal at high or "1".

3-Phase Write Transmission Cycle



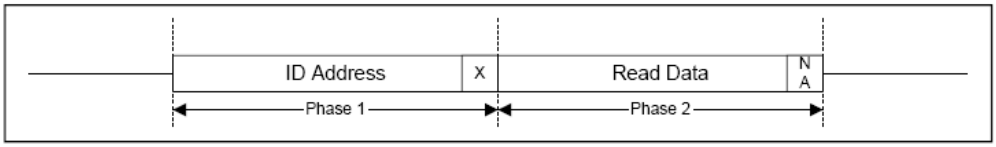
The 3-phase write transmission cycle is a full write cycle such that the master can write one byte of data to a specific slave(s). The ID address identifies the specific slave that the master intends to access. The sub-address identifies the register location of the specified. The write data contains 8-bit data that the master intends to overwrite the content of this specific address. The 9th bit of the three phases will be Don't-Care bits.

2-Phase Write Transmission Cycle



The 2-phase write transmission cycle is followed by a 2-phase read transmission cycle. The purpose of issuing a 2-phase write transmission cycle is to identify the sub-address of some specific slave from which the master intends to read data for the following 2-phase read transmission cycle. The 9th bit of the two write transmission phases will be Don't-Care bits.

2-Phase Read Transmission Cycle



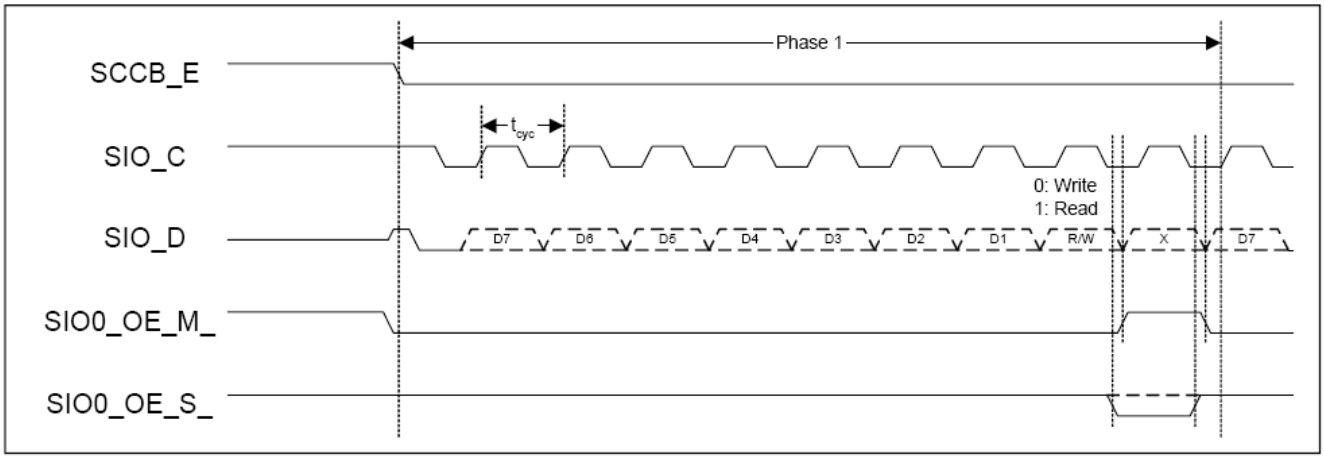
There must be either a 3-phase or a 2-phase write transmission cycle asserted ahead of a 2-phase read transmission cycle. The 2-phase read transmission cycle has no ability to identify the sub-address. The 2-phase write transmission cycle contains read data of 8 bits and a 9th, NA bit. The master must drive the NA bit at logical 1.

Phase 1

Phase 1 is asserted by the master to identify the selected slave to which data is read or written. Each slave has a unique ID address. The ID address is comprised of 7 bits, ordered from bit 7 to bit 1, and can identify up to 128 slaves. The 8th, bit, bit 0, is the read/write selector bit that specifies the transmission direction of the current cycle. A logical 0 represents a write cycle and a logical 1 represents a read cycle.

***ID address : (60)h**

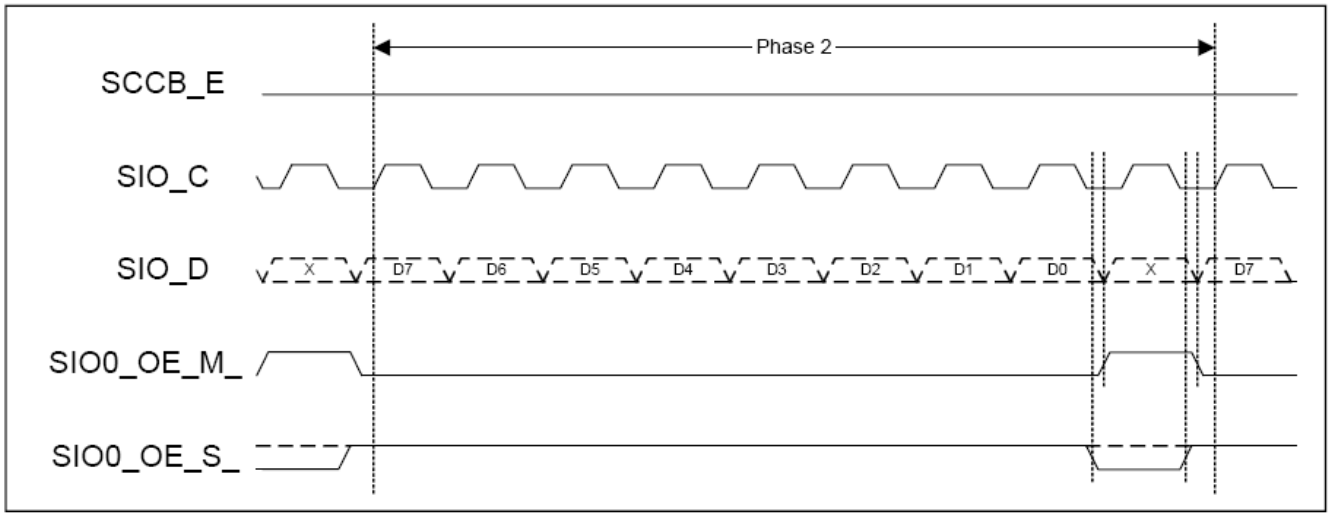
Phase 1 ID Address



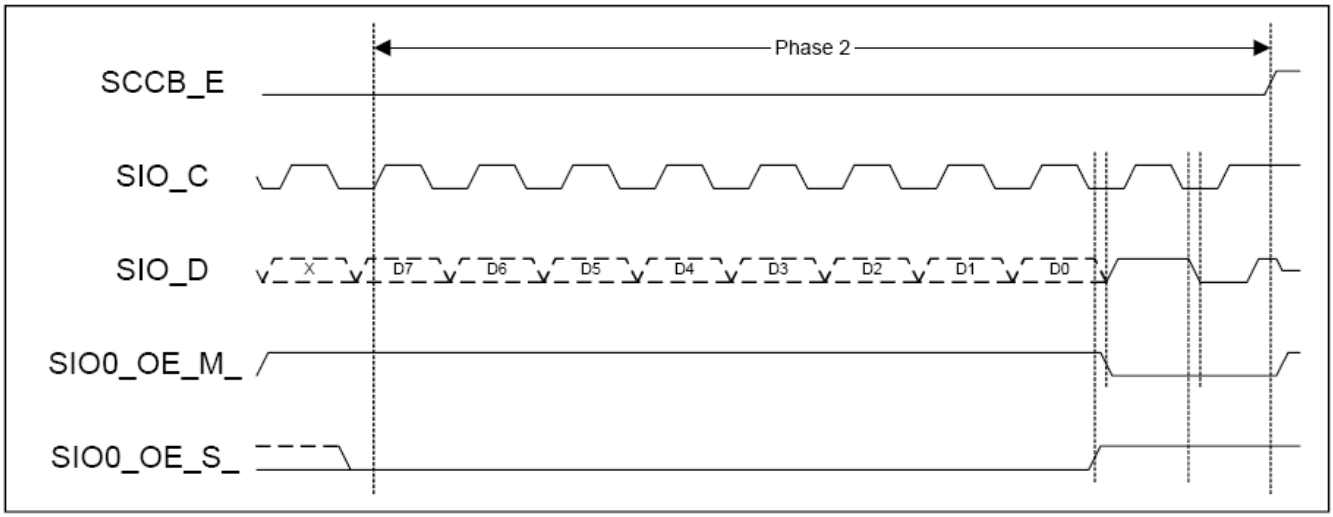
Phase 2

Either the master or the slave(s) may assert a phase 2 transmission. A phase 2 transmission asserted by the master identifies the sub-address of the slave(s) the master intends to access. A phase 2 transmission asserted by the slave(s) indicates the read data that the master will receive. The slave(s) recognize the sub-address of this read data according to previous 3-phase or 2-phase write transmission cycles.

Phase 2 Sub-address (3-Phase Write Transmission)



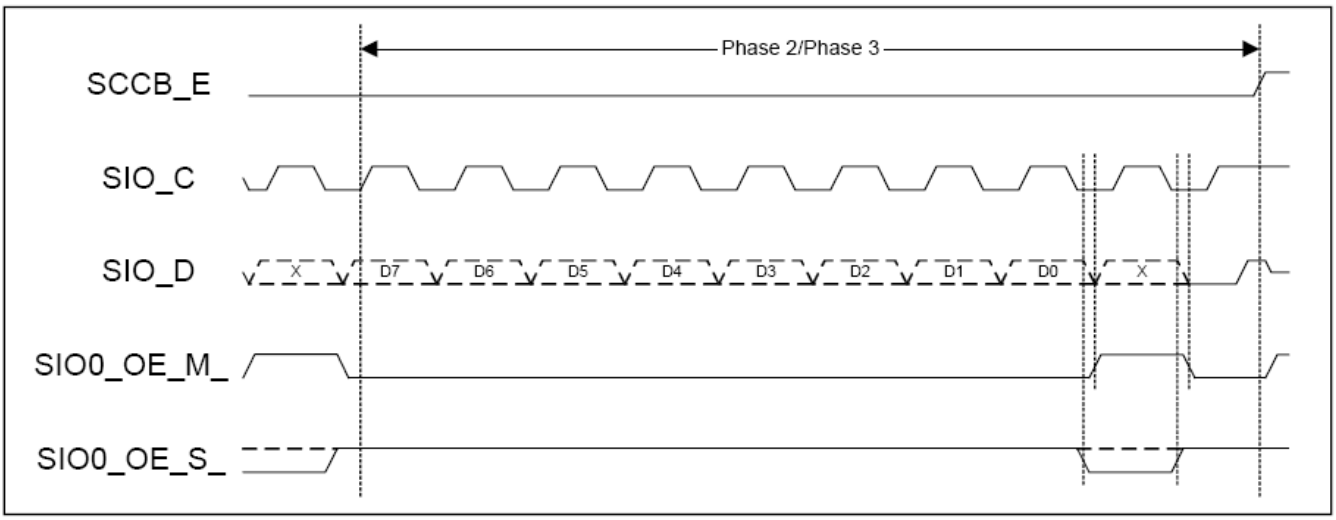
Phase 2 Read Data (2 Phase Read Transmission)



Phase 3

Only the master may assert the phase 3 transmission. The phase 3 transmission contains the actual data the master intends to write to the slave(s). The timing diagram is for both the Phase 2 sub-address write transmission and the Phase 3 write data transmission.

Phase 2/3 - Phase 2 Sub-address Write Transmission, Phase 3 Write Data Transmission

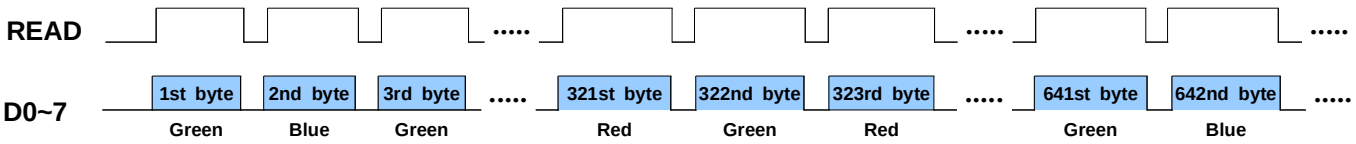


10. Data Format

10-1. RAW DATA FORMAT

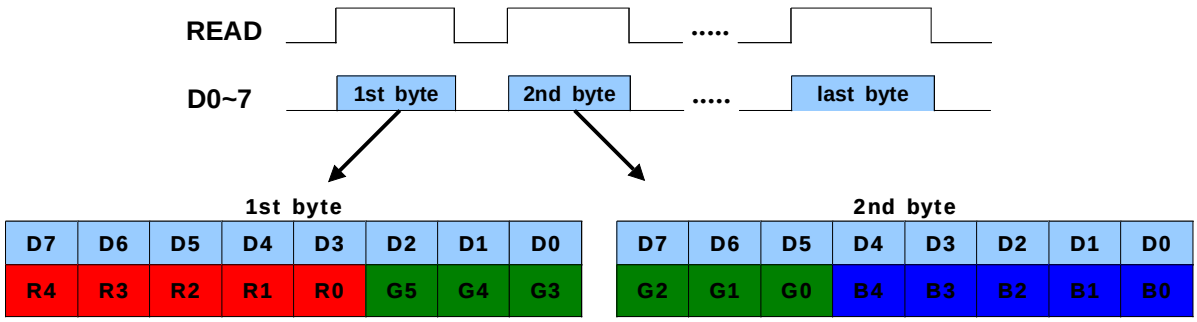
	1st byte	2nd byte	3rd byte	4th byte	5th byte	6th byte	7th byte	8th byte	9th byte	
1st line	G	B	G	B	G	B	G	B	G	...
2nd line	R	G	R	G	R	G	R	G	R	...
3rd line	G	B	G	B	G	B	G	B	G	...
4th line	R	G	R	G	R	G	R	G	R	...
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	

ex) QVGA(320*240) Raw Data Format



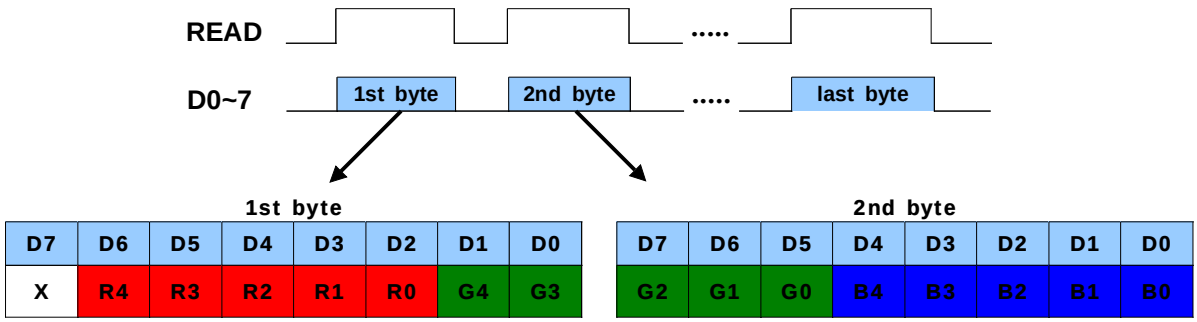
Total Byte : 320*240 = 76,800bytes / 1frame

10-2. RGB565 FORMAT



EX) QVGA(320*240) Total Byte : 320*240*2 = 153,600bytes / 1frame

10-3. RGB555 FORMAT



EX) QVGA(320*240) Total Byte : 320*240*2 = 153,600bytes / 1frame

11. Camera Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC - Gain control gain setting Range: [00] to [3F]
01	BLUE	80	RW	AWB - Blue channel gain setting Range: [00] to [FF]
02	RED	80	RW	AWB - Red channel gain setting Range: [00] to [FF]
03	VREF	4A	RW	Reference Voltage Control Bit[7:4]: Reserved Bit[3:2]: VREF end low 2 bits (high 8 bits at VSTOP[7:0] Bit[1:0]: VREF start low 2 bits (high 8 bits at VSTRT[7:0]
04	COM1	00	RW	Common Control 1 Bit[7]: Format selection (effective when COM3[7] = 1) 0: HSYNC timing for VGA series (SXGA, VGA, QVGA, and QQVGA) 1: HSYNC timing for CIF series (CIF, QCIF, and QQCIF) Bit[6]: CCIR656 format Bit[5]: 160 x 120 format. Effective only when QVGA output is selected (register bit COM7[4]) and related HREF skip mode based on format is selected (register COM1[3:2]) Bit[4]: 80 x 60 format. Effective only when QVGA output is selected (register bit COM7[4]) and related HREF skip mode based on format is selected (register COM1[3:2]) Bit[3:2]: HREF skip option 00: No skip 01: YUV/RGB skip every other row for YUV/RGB, skip 2 rows for every 4 rows for Raw data 1x: Skip 3 rows for every 4 rows for YUV/RGB, skip 6 rows for every 8 rows for Raw data Bit[1:0]: AEC low 2 LSB
05	BAVE	00	RW	U/B Average Level Automatically updated based on chip output format
06	GEAVE	00	RW	Y/Ge Average Level Automatically updated based on chip output format
07	GOAVE	00	RW	Y/GO Average Level Automatically updated based on chip output format
08	RAVE	00	RW	V/R Average Level Automatically updated based on chip output format

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COM2	01	RW	Common Control 2 Bit[7]: Internal use only. Use electrical BLC instead of optical BLC Bit[6]: Internal use only. SA1 always short Bit[5]: Test mode Bit[4]: Soft sleep mode Bit[3:2]: Internal use only. Long RST option Bit[1:0]: Output Drive Select 00: 1x 01: 2x 10: 2x 11: 4x
0A	PID	96	R	Product ID Number MSB (Read only)
0B	VER	48	R	Product ID Number LSB (Read only)
0C	COM3	00	RW	Common Control 3 Bit[7]: MODSEP, used for internal check 0: SA1 timing and HSYNC timing changes automatically when format changes 1: SA1 timing controlled by COM9[5] and HSYNC timing controlled by COM1[7] Bit[6]: Output data MSB and LSB swap Bit[5]: Precharge Blue line option Bit[4]: Sampling Blue line option Bit[3]: Pin selection 1: Change RESET pin to EXPST_B (frame exposure mode timing) and change PWDN pin to FREX (frame exposure enable) Bit[2]: Output 2 pixel average enable (used for sub-sampling mode) Bit[1]: Pre-charge source follower gate voltage set to VDD Bit[0]: Single frame output (used for Frame Exposure mode only)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0D	COM4	40	RW	Common Control 4 Bit[7]: Output 4 pixel average enable (used for sub-sampling mode) Bit[6]: Bypass anti-blooming circuits Bit[5]: Bypass analog BLC circuits Bit[4]: Analog clock generation non-overlap clock option 0: Normal current 1: Additional 2 ns non-overlay (effective only when COM4[3] is high) Bit[3]: Use analog clock generation non-overlap instead of digital generation Bit[2]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[1]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[0]: Set SA1 always enable when set to high
0E	COM5	01	RW	Common Control 5 Bit[7]: System clock selection. If the system clock is 48 MHz, this bit should be set to high to get 15 fps for YUV or RGB Bit[6]: EQ and SP non-overlap option 0: 3 ns 1: 5 ns Bit[5]: AD clock adds some delay to EQ 50 Bit[4]: Slam mode (used for slave mode) Bit[3]: ADC offset manual control 0: Offset is controlled automatically 1: Register OFON[7:4] can enable ADC offset addition Bit[2]: Enable SA1 capacitor pre-charge to VrHi Bit[1]: Manual control 1 line AEC Bit[0]: Exposure step can be set longer than VSYNC time 1: In Normal mode, AEC changes by 1/16 and in Fast mode, AEC changes by double
0F	COM6	43	RW	Common Control 6 Bit[7]: Output of optical black line option 1: Enable HREF at optical black Bit[6]: BLC input selection 0: Use electrical black line as BLC signal 1: Use optical black line as BLC signal Bit[5]: B/R in two different channels Bit[4]: HREF is high from optical black line Bit[3]: Enable bias for ADBLC Bit[2]: ADBLC offset 0: Use 4-channel ADBLC 1: Use 2-channel ADBLC Bit[1]: Reset all timing when format changes Bit[0]: Enable ADBLC option

Address (Hex)	Register Name	Default (Hex)	R/W	Description
10	AECH	40	RW	Exposure Value - high 8 MSB
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7]: Digital PLL option 1: Enable double clock option, meaning the maximum PCLK can be as high as input clock Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar Range: [0 0000] to [1 1111]
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Output format - VGA selection Bit[5]: Output format - CIF selection Bit[4]: Output format - QVGA selection Bit[3]: Output format - QCIF selection Bit[2]: Output format - RGB selection Bit[1]: Internal use only (color bar) Bit[0]: Output format - Raw RGB (COM7[2] must be set high)
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit (used only in fast condition and COM5[0] is low) 0: Fast condition change maximum step is VSYNC 1: Unlimited step size Bit[5]: Banding filter ON/OFF Bit[4]: Banding filter automatic option 1: Input clock can be 12 MHz. Bit[3]: Enable AEC time can be less than 1 line option Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COM9	4A	RW	Common Control 9 Bit[7:6]: Automatic Gain Ceiling - maximum AGC value 00: 2x 01: 4x 1x: 8x Bit[5]: SA1 pre-charge and sampling option for address skip mode (effective only when COM3[7] = 1) 0: SA1 timing for full resolution 1: SA1 timing for address skip mode Bit[4]: SA1 timing option for average Bit[3]: Exposure timing can be less than limit of banding filter when light is too strong Bit[2]: Data format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than VSYNC Bit[0]: Freeze AGC/AEC
15	COM10	00	RW	Common Control 10 Bit[7]: Set pin definition 1: Set RESET to SLHS (slave mode horizontal sync) and set PWDN to SLVS (slave mode vertical sync) Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 1: No PCLK output when HREF is low Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: Reset signal end point option Bit[1]: VSYNC negative Bit[0]: HSYNC negative
16	WS	00	RW	Black Sun Cancel Option Bit[7:4]: Automatic offset adjustment for ADC threshold Bit[3]: Black sun cancel option ON/OFF Bit[2:0]: Black sun cancel option reference (for internal use only)
17	HSTART	24	RW	Output Format - Horizontal Frame (HREF column) start high 8-bit (low 3 bits are at HREF[2:0])
18	HSTOP	C4	RW	Output Format - Horizontal Frame (HREF column) end high 8-bit (low 3 bits are at HREF[5:3])
19	VSTRT	01	RW	Output Format - Vertical Frame (row) start high 8-bit (low 2 bits are at VREF[1:0])
1A	VSTOP	F1	RW	Output Format - Vertical Frame (row) end high 8-bit (low 2 bits are at VREF[3:2])
1B	PSHFT	00	RW	Data Format - Pixel Delay Select (delays timing of the Y[9:0] data relative to HREF in pixel units) Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1C	MIDH	7F	R	Manufacturer ID Byte - High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte - Low (Read only = 0xA2)
1E	DLY	00	RW	Signal Delay Bit[7:3]: Reserved Bit[2]: Enable digital black sun cancel option Bit[1:0]: Delay adjustment for digital black sun cancel option. This delay is used for internal debug.
1F	LAEC	00	RW	Exposure time of less than 1 line, the count is in pixel number
20	BOS	80	RW	B Channel ADBLC Result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range (high 7 bits)
21	GBOS	80	RW	Gb channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10 bit range
22	GROS	80	RW	Gr channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10 bit range
23	ROS	80	RW	R channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10 bit range
24	AEW	78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	68	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: Upper limit of 4 MSB Bit[3:0]: Lower limit of 4 LSB
27	BBIAS	80	RW	B Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10 bit range

Address (Hex)	Register Name	Default (Hex)	R/W	Description
28	GbBIAS	80	RW	Gb Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10 bit range
29	GrBIAS	80	RW	Gr Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10 bit range
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7:4]: 4 MSB for dummy pixel insert in horizontal direction Bit[3:2]: HSYNC falling edge delay 2 MSB Bit[1:0]: HSYNC rising edge delay 2 MSB
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	RBIAS	80	RW	R Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10 bit range
2D	ADVFL	00	RW	LSB of insert dummy lines in vertical direction (1 bit equals 1 line)
2E	ADVFH	00	RW	MSB of insert dummy lines in vertical direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	HSYST	08	RW	HSYNC Rising Edge Delay (low 8 bits)
31	HSYEN	30	RW	HSYNC Falling Edge Delay (low 8 bits)
32	HREF	24	RW	HREF Control Bit[7:6]: HREF edge offset to data output Bit[5:3]: HREF end 3 LSB (high 8 MSB at register HSTOP) Bit[2:0]: HREF start 3 LSB (high 8 MSB at register HSTART)
33	CHLF	00	RW	Array Current Control Bit[7:6]: Total current for array Bit[5]: SA1HLF (SA1 current half option) Bit[4]: BIT2X (bit line current double) Bit[3]: CAPsel (pin selection for VcCHG) 0: Used for VcCHG 1: Used for HVDD Bit[2]: PIHLF (half current option for OPAM in SA1) Bit[1]: Half current option for analog Bit[0]: Half current option for ADC

Address (Hex)	Register Name	Default (Hex)	R/W	Description
34	ARBLM	03	RW	Array Reference Control Bit[7]: Soft reset option for array Bit[6:4]: Anti-blooming reference voltage control Bit[3]: PMOS feedback for pre-charge voltage Bit[2:0]: Current selection for OPAM of pre-charge reference
35	VRHL	90	RW	Array Reference Voltage for SA1 capacitor Bit[7]: Set VrHi reference to VDD Bit[6:5]: VrHi reference voltage Bit[4]: Set VrLow reference to GND Bit[3:2]: VrLow reference voltage Bit[1]: Power down diode reference voltage circuits Bit[0]: Enable band gap reference instead of diode reference
36	VIDO	49	RW	Diode Reference Voltage Adjustment Bit[7]: Low current voltage to DVDD at power down (for internal use only) 0: Power down will result in no voltage to DVDD 1: Provides low current voltage to DVDD at power down Bit[6:4]: Pre-charge voltage adjust when Hard reset mode is used Bit[3:0]: Diode reference voltage adjustment
37	ADC	04	RW	ADC Control Bit[7]: ADC clock for PH1 and PH2 non-overlap delay option 1: 2 ns more delay Bit[6]: ADC clock for PH1 and PH1_0 delay option 1: 2 ns more delay Bit[5:4]: ADC reference for comparator adjustment Bit[3]: ADC range adjustment 0: 1x range 1: 1.5x range Bit[2:0]: ADC range adjustment 000:0.8x 100:1x 111: 1.2x
38	ACOM	12	RW	ADC and Analog Common Mode Control Bit[7]: 2x gain for analog Bit[6:5]: Common mode control for analog OPAM Bit[4]: ADC reference control Bit[3:2]: ADC offset adjustment Bit[1:0]: Common mode control for ADC OPAM

Address (Hex)	Register Name	Default (Hex)	R/W	Description
39	OFON	00	RW	ADC Offset Control Bit[7:4]: Enable Gb, Gr, B, R channel ADC offset addition (effective only when COM5[3] = 1) Bit[3]: Set reset signal for first of two dummy lines (see bit[2] definition below) 0: Reset always low 1: Reset always high Bit[2]: Set reset signal for second of two dummy lines (see bit[3] definition above) 0: Reset always low 1: Reset always high Bit[1:0]: Source follower for array to analog current control 00: Maximum 11: Minimum
3A	TSLB	0C	RW	Line Buffer Test Option Bit[7:6]: Line buffer selection (only effective in Raw data output mode) 00: Use current data as output 01: Use line buffer 1 as output 10: Use line buffer 2 as output 11: Use line buffer 3 as output Bit[5]: Bit reverse option 1: Bit reverse option for output signal (e.g., 0110 0111 becomes 1001 1000) Bit[4]: UV output value 1: Use fixed UV value set in registers MANU and MANV as UV output instead of chip output Bit[3]: Output sequence is Y U Y V instead of U Y V Y Bit[2]: Output sequence is Y V Y U instead of Y U Y V Bit[1:0]: Double clock option
3B	COM11	80	RW	Common Control 11 Bit[7]: Night mode option 1: Frame rate will adjust based on COM11[6:5] before AGC gain increases more than 2. Also, ADVFL and ADVFL will be automatically updated. Bit[6:5]: Night mode insert frame option 00: No dummy frames 01: Maximum 1 frame 10: Maximum 3 frames 11: Maximum 7 frames Bit[4:3]: Average calculation window option 00: Use full frame 01: Use half frame 10: Use quarter frame 11: Use lower two-thirds Bit[2]: AWB algorithm option Bit[1]: AWB debug mode Bit[0]: Manual banding filter mode

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3C	COM12	40	RW	Common Control 12 Bit[7]: HREF option 0: No HREF when VREF is low 1: Always has HREF Bit[6:5]: BLC option for Blue 00: Both Red and Blue do BLC 01: Only Red line does BLC 10: Only Blue line does BLC 11: Not allowed Bit[4]: Address skip option for CIF, QVGA, and QCIF (for internal use only) Bit[3]: Interpolation option (for internal use only) Bit[2]: Enable YUV average Bit[1:0]: EQ and SP delay option for analog circuits (for internal use only)
3D	COM13	99	RW	Common Control 13 Bit[7:6]: Gamma selection for signal 00: No gamma function 01: Gamma used for Y channel only 10: Gamma used for Raw data before interpolation 11: Not allowed Bit[5]: RGB average enable Bit[4]: Enable color matrix for RGB or YUV Bit[3]: Enable Y channel delay option Bit[2:0]: Output delay related to HREF option
3E	COM14	0E	RW	Common Control 14 Bit[7]: PLL option 1: Disable PLL in chip Bit[6]: Bypass PLL Bit[5]: Use PLL clock as input clock instead of pin input clock Bit[4]: Used for array reference to clamp signal Bit[3]: Interpolation option 1: Use weight interpolation instead of average Bit[2]: Y interpolation uses 8 neighbor G instead of 4. Bit[1]: Enable edge enhancement for YUV output (effective only for YUV/RGB, no use for Raw data) Bit[0]: Edge enhancement option 1: Double edge enhancement factor
3F	EDGE	88	RW	Edge Enhancement Adjustment Bit[7:4]: Edge enhancement threshold Bit[3:0]: Edge enhancement factor

Address (Hex)	Register Name	Default (Hex)	R/W	Description
40	COM15	C0	RW	Common Control 15 Bit[7:6]: Data format - output full range enable 00: Output range: [00] to [FF] 01: Output range: [01] to [FE] 1x: Output range: [10] to [F0] Bit[5:4]: RGB 555/565 option (must set COM7[2] high) x0: Normal RGB output 01: RGB 565 11: RGB 555 Bit[3]: In RGB 555/565 format, R and B swap Bit[2:1]: Frame exposure time option (used for debug only) Bit[0]: Low pass filter for BLC OFF/ON 0: ON 1: OFF
41	COM16	00	RW	Common Control 16 Bit[7]: SA1 enable option 1: No SA1 enable Bit[6]: SA1 always enabled at frame exposure Bit[5:2]: Frame exposure option (used for debug only) Bit[1]: Color matrix coefficient double option Bit[0]: RB average option for interpolation
42	COM17	08	RW	Common Control 17 Bit[7]: B channel pre-gain Bit[6]: R channel pre-gain Bit[5]: Analog block selection (used for debug only) Bit[4]: Edge enhancement option (used for debug only) Bit[3]: Enable anti-gamma function Bit[2]: Select single frame out Bit[1]: Tri-state output Bit[0]: AGC maximum gain 16x
43	AWBTH1	F0	RW	AWB Threshold 1
44	AWBTH2	14	RW	AWB Threshold 2
45	AWBTH3	40	RW	AWB Threshold 3
46	AWBTH4	68	RW	AWB Threshold 4
47	AWBTH5	30	RW	AWB Threshold 5
48	AWBTH6	70	RW	AWB Threshold 6
49-4E	RSVD	XX	-	Reserved
4F	MTX1	58	RW	Matrix Coefficient 1
50	MTX2	48	RW	Matrix Coefficient 2
51	MTX3	10	RW	Matrix Coefficient 3
52	MTX4	28	RW	Matrix Coefficient 4

Address (Hex)	Register Name	Default (Hex)	R/W	Description
53	MTX5	48	RW	Matrix Coefficient 5
54	MTX6	70	RW	Matrix Coefficient 6
55	MTX7	40	RW	Matrix Coefficient 7
56	MTX8	40	RW	Matrix Coefficient 8
57	MTX9	40	RW	Matrix Coefficient 9
58	MTXS	0F	RW	Matrix Coefficient Sign for coefficient 9 to 2 0: Plus 1: Minus
59	AWBC1	5E	RW	AWB CWF Definition Option 1
5A	AWBC2	F1	RW	AWB CWF Definition Option 2
5B	AWBC3	32	RW	AWB CWF Definition Option 3
5C	AWBC4	70	RW	AWB CWF Definition Option 4
5D	AWBC5	86	RW	AWB CWF Definition Option 5
5E	AWBC6	1E	RW	AWB CWF Definition Option 6
5F	AWBC7	15	RW	AWB CWF Definition Option 7
60	AWBC8	0A	RW	AWB CWF Definition Option 8
61	AWBC9	4B	RW	AWB Option
62	LCC1	00	RW	Lens Correction Option 1
63	LCC2	00	RW	Lens Correction Option 2
64	LCC3	10	RW	Lens Correction Option 3
65	LCC4	80	RW	Lens Correction Option 4
66	LCC5	00	RW	Lens Correction Option Bit[7:4]: Reserved Bit[3:1]: Lens correction parameter output Bit[0]: Lens correction enable
67	MANU	80	RW	Manual U Value (effective only when register TSLB[4] is high)
68	MANV	80	RW	Manual V Value (effective only when register TSLB[4] is high)
69	HV	00	RW	Reference for Black Sun Cancel Option Bit[7:4]: Reference for black sun cancel option Bit[3]: Reserved Bit[2:1]: MSB of manual banding filter Bit[0]: Matrix coefficient 1 sign
6A	MBD	00	RW	LSB Manual Banding Filter Value (effective only when COM11[0] is high). 10-bit value is the minimum value possible when register bit COM11[0] is enabled. After that, AEC will double on the basis of that value.

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6B	DBLV	3A	RW	Charge Pump Option Bit[7]: Bypass charge pump and use AVDD for RST Bit[6:4]: Charge pump adjustment Bit[3:0]: Band gap reference adjustment
6C-7B	GSP	XX	RW	Sixteen different slop points for 16 linear of Gamma curve
7C-8A	GST	XX	RW	Fifteen different starting points for 16 linear of Gamma curve
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

12. Dimensions

27 * 48 * 7.5 mm(Except Connector)