AC Line Monitoring Using the Si890x Family of Isolated ADCs

1. Introduction

Measurement and control applications commonly use analog-to-digital converters (ADCs) to make precise measurements of key system parameters, such as voltage and current. For best noise performance, the analog signal must be immediately digitized at the analog sensor output and conditioned (i.e. filtered) in the digital domain by a DSP or MCU. In many cases, the end application can have some combination of local high voltage, floating grounds, or problematic ground noise, all of which can be resolved by the use of galvanic isolation.

The Silicon Labs' Si890x Monitoring ADC family integrates a 10-bit SAR ADC (2 µs conversion time) with a 5 $kVAC_{RMS}$ isolated UART (Si8900), I^2C (Si8901) or SPI (Si8902) serial port, resulting in a single package, isolated ADC solution. This application note discusses the Si890x in an isolated ac line monitor application that measures 110/240 VAC line voltage and current and uses isolation for both signal level shifting and safety.

2. System Diagram

Figure 1 shows the ac line monitor system top-level block diagram, which is composed of three functional blocks: the Si8902 isolated ADC (SPI serial port), an input-side ac line-derived power supply circuit (2.7 V to 3.6 V at 15 mA max), and an ac line interface circuit that transforms the ac line voltage/current input into a 3 Vp-p(max) signal centered around a fixed offset voltage of 1.5 VDC.

Referring to Figure 2, The ac line neutral is used as the ground reference for the Si8902 input-side. AC line current is sensed through the parallel shunt resistor combination of R16,R17 and R18. AC line voltage is sensed through a voltage attenuator consisting of R5, R6, R7, R8, R9, and R10. The on-chip ADC digitizes these analog line signals and transmits the converted data through the on-chip isolator to the on-chip serial port where it can be read by the user's host processor (typically an MCU).

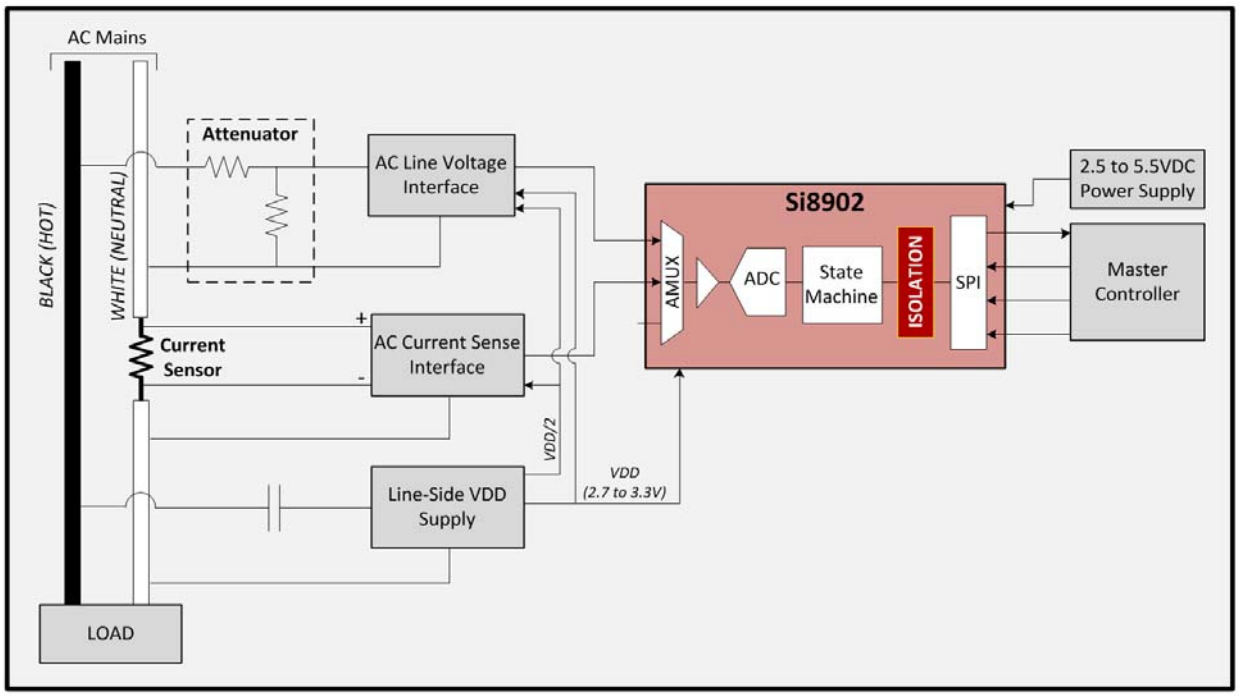


Figure 1. Top-Level AC Line Monitor Block Diagram

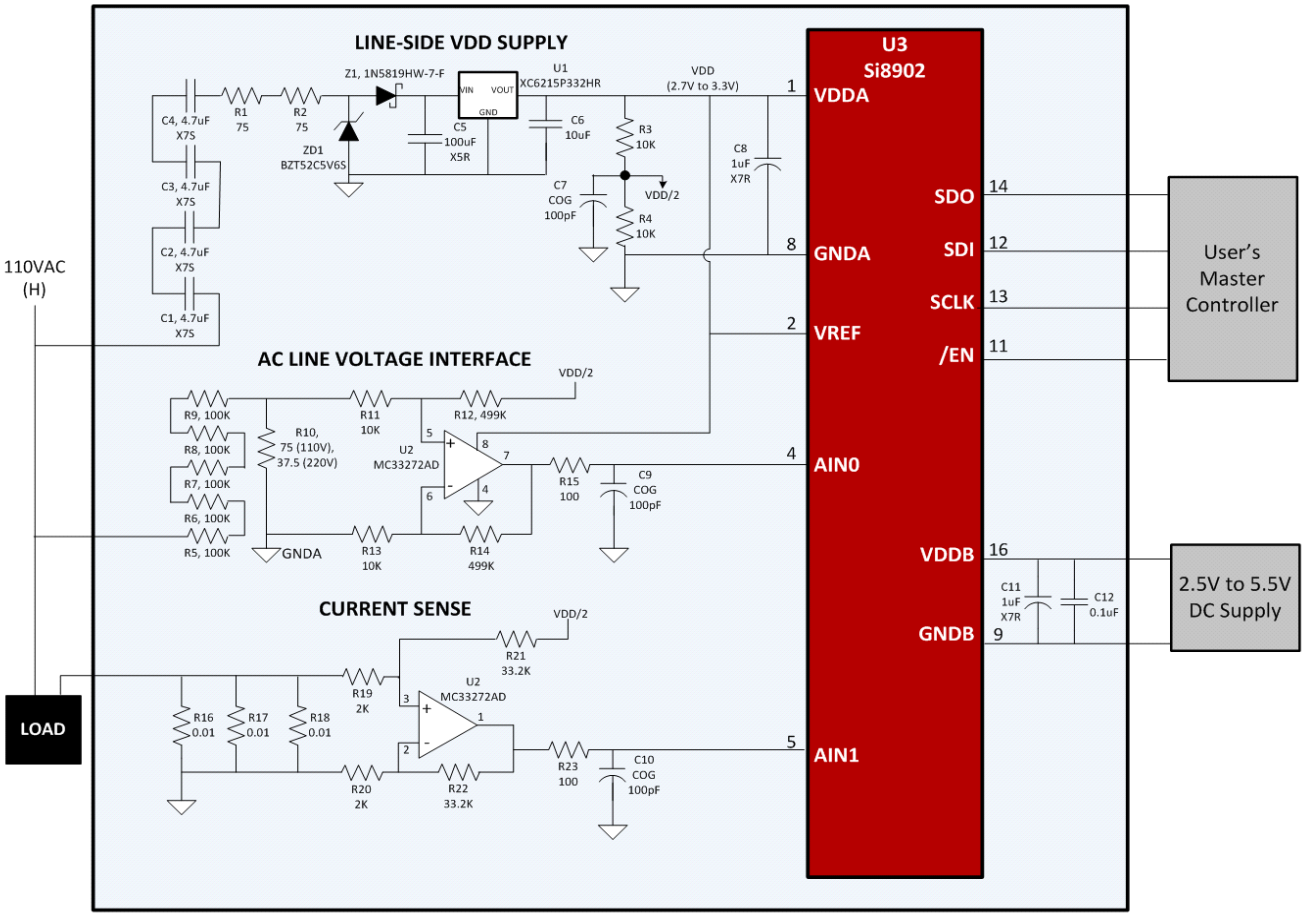


Figure 2. AC Line Monitor Schematic

3. Design Considerations

For best results, the Si890x should be placed in a low-noise area of the board and powered from a clean, well-bypassed V_{DD} source. Care must be taken to avoid noise coupling into the RESET pin, and the ADC inputs must have anti-aliasing capacitors installed from each ADC input to ground in close proximity to the Si890x. In addition, the user must adhere to the hardware guidelines detailed in the following paragraphs below.

3.1. Power-On Reset

While the Si890x internal power-on reset circuit eliminates the need for external reset circuits, the user may reset the Si890x externally by momentarily grounding the $\overline{RST}$ input if so desired. If the Si890x is operated in an electrically noisy environment, it is highly recommended that a 2 kΩ resistor from $\overline{RST}$ to V_{DD} be added to guard against erroneous reset events due to noise coupling into the $\overline{RST}$ input.

3.2. Supply Bypass

AC line-side circuits can be powered by the line-side Vdd supply shown at the top of Figure 2 or from a local external supply. See the Si890x data sheet for details. All Vdd inputs must be bypassed with a 1.0 µF capacitor and located as close as possible to the Si890x Vdd pins. When using the Si8902, the serial port side Vdd bypass capacitor should be located as close to package pin 10 as possible.

3.3. Serial Port Bit Rates

The Si8901 (I^2C) and Si8902 (SPI) serial port bit rates are determined by master's clock signal. For example, a 200 kHz master clock signal on the Si8901 SCL input results in a communications bit rate of 200 kbps. The Si8900 (UART) automatically adapts to the bit rate used by the master. For more information, see “AN635: Si8900 Automatic Baud Rate Detection” available for download at www.silabs.com/isolation.

3.4. Si8901 Bus Pullups

When using the Si8901, a 5 kΩ pull-up resistor must be installed from the SDA pin to Vdd, as stated in the data sheet. The slave address of Si8901 is set to “F0” and is not user-programmable. For more information about the I^2C address, contact Silicon Labs.

3.5. Current Sense Resistor Value

The current sense resistor value must conform to the following equation:

$$R_0 \times I_{Max} \times G_V = V_{ADC}$$

where R_0 is the current sensing shunt resistor value; I_{Max} is the maximum measurable peak current; G_V is the gain of amplifier, and V_{ADC} is the ADC input range (0 ~ V_{Ref}) determined by the ADC reference voltage V_{Ref}. Si890x can select V_{Ref} = Vdd or external V_{Ref} voltage connecting to the V_{Ref} pin.

3.6. Voltage Sense Resistor Values

The voltage sense resistor values must conform to the following equation:

$$VI_{Max} \times \frac{R_{10}}{R_{10} + R_{5,6,7,8,9}} \times G_V = V_{ADC}$$

where VI_{Max} is the maximum measurable peak voltage; G_V is the gain of amplifier, and V_{ADC} is the ADC input range determined by the ADC reference voltage (V_{Ref} = 2.7 V in this example).

3.7. Other Recommendations

Referring to Figure 2, care must be taken to ensure that the values of op-amp input resistors R_{11}, R_{13}, R_{19}, and R_{20} do not significantly load the voltage divider resistor R_{10} and the parallel combination of current shunt resistors R_{16}, R_{17}, R_{18}. The resistor value ratio must be selected based on the measurement accuracy needs of the end application. The schematic in Figure 2 uses a ratio of 100x. Note that higher ratio values decrease loading effects but increase noise, thereby lowering measurement accuracy. The user must choose the best compromise for the application at hand. In addition, R_{11} and R_{13} must be in the range of hundreds of kΩ since R_{10} and feedback resistor R_{14} will both be in the kΩ range. In some cases, the output of U2 Pin 7 may be subjected to high resistor thermal noise, which is positively proportional to the resistance value. In the worst case, a large value resistor in the op-amp feedback loop may cause oscillation, which is resolved by placing a 1.2 nF capacitor across R_{14}. C_9, C_{10}, R_{15}, and R_{23} are anti-alliance filters, and their values depend on the frequency range of interest. Resistors R_{15} and R_{23} are recommended to be 100 Ω, and the values of C_9 and C_{10} can be adjusted to meet the user's frequency band requirement.

3.7.1. Layout Considerations

A low-cost, two-layer board may be used where open spaces are filled with ground and Vdd on each side of the board for better signal grounding and heat dissipation. Separation between the high-voltage and low-voltage areas of the board should follow the recommendations outlined in the Si890x data sheet. Discrete components should use a larger package, such as the 1206, for better power dissipation whenever board space allows. Ensure that the power, voltage, and current ratings of all components (including connectors) have the appropriate design margins. If desired, multiple components, such as resistors and capacitors, can be used in series or in parallel to increase their power rating. Current and voltage sensing components should be placed at the edge of the board and occupy the minimal space in the board. In particular, avoid placing them deep inside the PCB to avoid noise coupling.

4. System Performance

The performance data shown in Figure 3 was generated using the Si890x EVB (part number Si890xPWR-EVB) available from Silicon Labs and its affiliated distributors. This evaluation board demonstrates the operation of all three members of the Si890x isolated ADC family. Referring to Figure 3, the top two traces show the ac voltage waveform (blue trace) and the current waveform (yellow trace) at U3 Pin 4 and Pin 5 respectively (Figure 2). The ac voltage (green trace) and current (purple trace) in the lower two traces were converted by the ADC in U3, then converted back to analog by the D/A converter in the master controller.

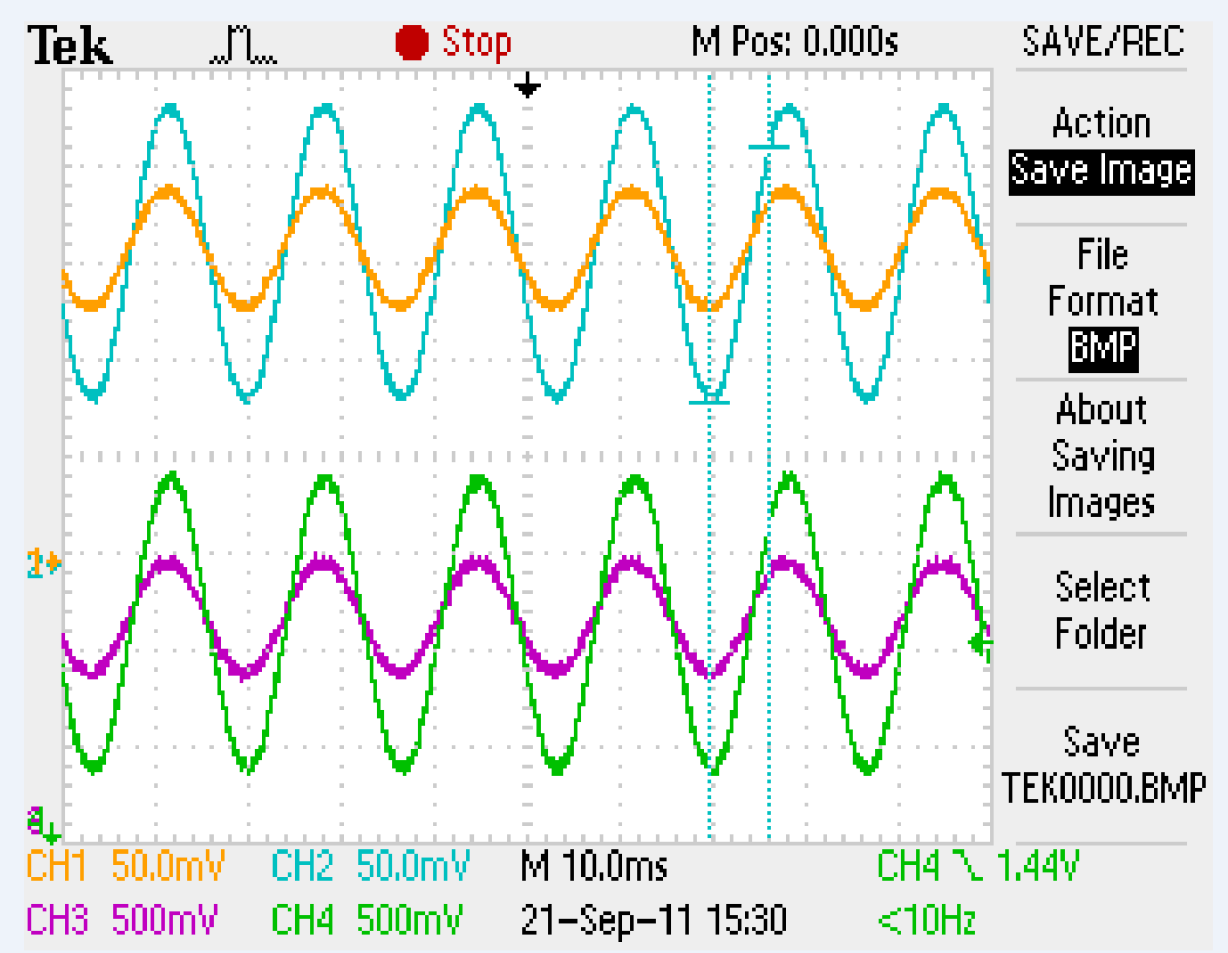
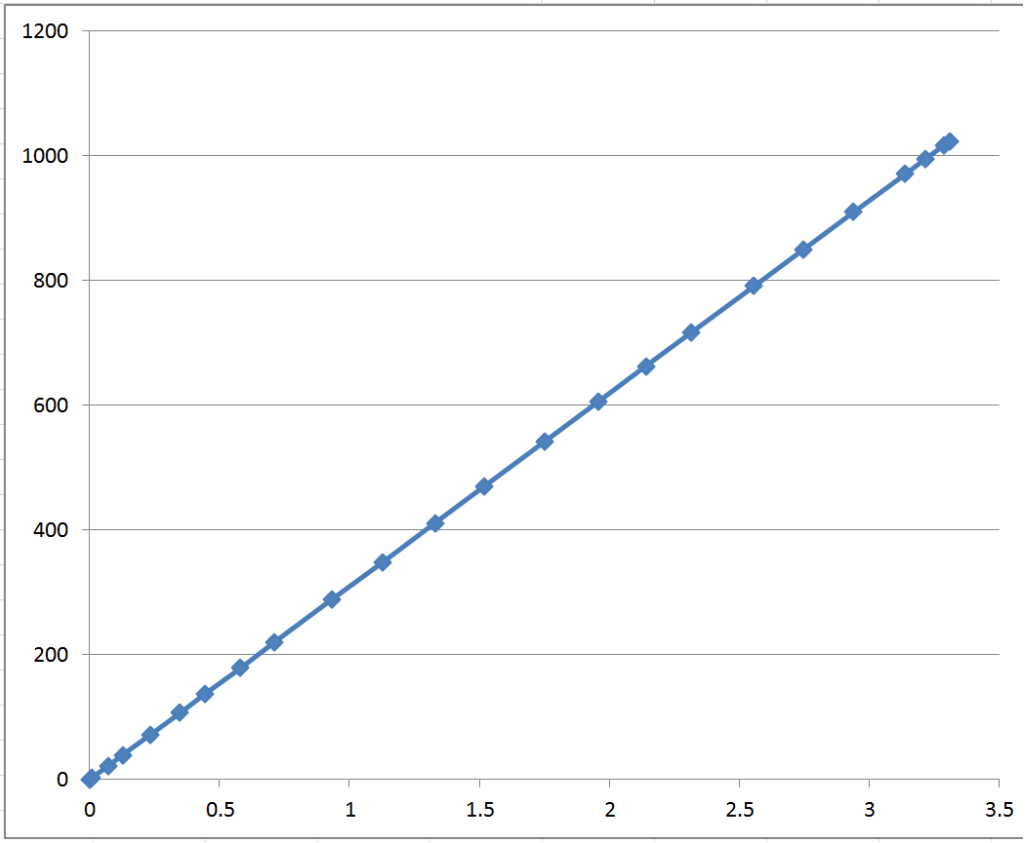


Figure 3. Typical AC Line Voltage and Current Monitoring Waveforms

Figure 4 shows the ADC measurement accuracy of the Si8900 (UART serial port) and Si8902 (SPI serial port) as measured on the Si890x EVB. In this measurement, the Si890x devices operate in Demand mode (on-demand ADC conversion) measuring variable dc levels through ADC MUX Channel 2.

	Vin (V)	data
2	0	0
3	0.011	3
4	0.074	22
5	0.128	39
6	0.236	72
7	0.349	107
8	0.446	137
9	0.58	179
10	0.713	220
11	0.935	289
12	1.128	348
13	1.33	411
14	1.52	470
15	1.753	542
16	1.96	606
17	2.142	662
18	2.314	716
19	2.557	791
20	2.747	850
21	2.94	910
22	3.138	971
23	3.217	995
24	3.289	1017
25	3.312	1023



	Vin (V)	data
2	0	0
3	0.003	2
4	0.025	10
5	0.136	50
6	0.325	123
7	0.455	172
8	0.655	248
9	0.735	279
10	1.108	420
11	1.575	597
12	1.815	687
13	2.247	850
14	2.489	942
15	2.588	978
16	2.698	1020
17	2.714	1023

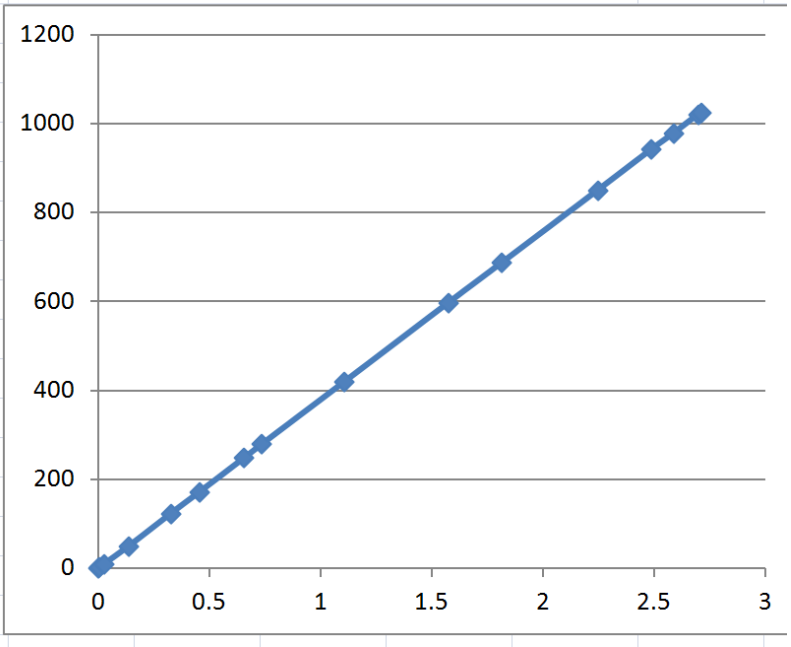


Figure 4. Demand Mode Data Measurement Through Channel 2 of the Si8900 and Si8902

5. References

- Silicon Laboratories, Inc., Si8900/1/2 data sheet.
- NXP UM102104, I^2C-bus specification and user manual, Rev. 03 - 19 June 2007
- SMBus.org, “System Management Bus (SMBus) Specification”, Version 2.0, August 3, 2000
- Silicon Laboratories, Inc., “AN635: Si8900 Automatic Baud Rate Detection”.

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