ATTACHMENT 2

AEC - Q100-002 REV-D

HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST
Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Counsel would especially like to recognize the following significant contributors to the development of this document:

Mark A. Kelly
Delphi Delco Electronics Systems
Change Notification

The following summary details the changes incorporated into AEC-Q100-002 Rev-D:

- **Section 3.5, steps d, e, j, and k:** Added wording to allow lower voltage level stressing (250 volt) for devices failing the 500 volt level.

- **Section 5, Acceptance Criteria:** Added wording to reflect device classification, rather than meeting a 2000 volt level.

- **Table 3, Integrated Circuit HBM ESD Classification Levels:** Added new table listing classification levels for HBM ESD.
METHOD - 002

HUMAN BODY MODEL (HBM)
ELECTROSTATIC DISCHARGE (ESD) TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for electronic devices.

1.2 Reference Documents

EOS/ESD Association Specification S5.1
JEDEC Specification EIA/JESD22/A114

1.3 Terms and Definitions

The terms used in this specification are defined as follows.

1.3.1 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 DUT

An electronic device being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD)

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity

An ESD voltage level resulting in device failure.
1.3.5 ESD Simulator

An instrument that simulates the human body model ESD pulse as defined in this specification.

1.3.6 Human Body Model (HBM) ESD

An ESD pulse meeting the waveform criteria specified in this test method.

1.3.7 Non-Supply Pins

All pins including, but not limited to, input, output, bi-directional, Vref, Vpp, clock, and “no connect” pins. These pins do not supply voltage and/or current to the device under test.

1.3.8 Power Pins

All power supply, external voltage source, and ground pins. All power pins that are metallically connected together on the chip or in the package shall be treated as one (1) power pin.

1.3.9 PUT

The pin under test.

1.3.10 Ringing current (IR)

The high frequency current oscillation usually following the pulse rise time.

1.3.11 Withstanding Voltage

The ESD voltage level at which, and below, the device is determined to pass the failure criteria requirements specified in section 4.

1.3.12 Worst-Case Pin Pair (WCP)

WCP is the pin pair representing the worst-case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket.

2. EQUIPMENT

2.1 Test Apparatus

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent HBM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 1, Figure 2, and Figure 3.
Figure 1: Typical Equivalent HBM ESD Circuit

Notes:
1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc.
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
4. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 volt, 500 ohm resistor with ±1% tolerance.
5. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
6. Reversal of terminals A and B to achieve dual polarity is not permitted.
7. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe

The current probe shall have a minimum bandwidth of 350 MHz and maximum cable length of 1 meter (Tektronix CT-1 or equivalent).

2.2.2 Evaluation Loads

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with ±1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst-case pin pair (WCP) while passing through the current probe as defined in section 2.2.1.
2.2.3 Oscilloscope

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 MHz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst-case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. Simulators not capable of producing the maximum voltage level shown in Table 1 shall be qualified to the highest voltage level possible. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 1000 volt level using the worst-case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst-case pin pair (WCP) using only the shorting wire per section 2.4.1. The worst-case pin pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at either the 1000 or 4000 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure

a. With the required DUT socket installed and with no device in the socket, attach a shorting wire in the DUT socket such that the worst-case pin pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 5 nanoseconds per division or less.

c. Initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.
g. Set the horizontal time scale of the oscilloscope at 100 nanoseconds per division or greater and initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

h. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

i. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

j. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

Table 1: HBM Waveform Specification

<table>
<thead>
<tr>
<th>Voltage Level (V)</th>
<th>Ipeak for Short, $I_{ps}$ (A)</th>
<th>Ipeak for 500 Ohm*, $I_{pr}$ (A)</th>
<th>Rise Time for Short, $t_r$ (ns)</th>
<th>Rise Time for 500 Ohm*, $t_{rr}$ (ns)</th>
<th>Decay Time for Short, $t_d$ (ns)</th>
<th>Ringing Current, $I_R$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>0.60 - 0.74</td>
<td>.375 - .55</td>
<td>2.0 - 10</td>
<td>5.0 - 25</td>
<td>130 - 170</td>
<td>15% of $I_{ps}$ and $I_{pr}$</td>
</tr>
<tr>
<td>2000</td>
<td>1.20 - 1.46</td>
<td>Not Applicable</td>
<td>2.0 - 10</td>
<td>Not Applicable</td>
<td>130 - 170</td>
<td>15% of $I_{ps}$ and $I_{pr}$</td>
</tr>
<tr>
<td>4000</td>
<td>2.40 - 2.94</td>
<td>Not Applicable</td>
<td>2.0 - 10</td>
<td>Not Applicable</td>
<td>130 - 170</td>
<td>15% of $I_{ps}$ and $I_{pr}$</td>
</tr>
<tr>
<td>8000</td>
<td>4.80 - 5.86</td>
<td>Not Applicable</td>
<td>2.0 - 10</td>
<td>Not Applicable</td>
<td>130 - 170</td>
<td>15% of $I_{ps}$ and $I_{pr}$</td>
</tr>
</tbody>
</table>

* The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.

2.5 Automated ESD Test Equipment Relay Verification

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.
Figure 2: HBM current waveforms through a shorting wire
3. PROCEDURE

3.1 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall be stressed at one (1) voltage level using all pin combinations specified in Table 2. The use of a new sample group for each pin combination specified in Table 2 is also acceptable. Voltage level skipping is not allowed. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level. Therefore, the minimum number of devices required for ESD qualification is 3 devices, while the maximum number of devices depends on the number of pin combinations and the number of voltage steps required to achieve the maximum withstanding voltage. For example, a device (1 VCC pin, 1 GND pin, and 2 IO pins) with a maximum withstanding voltage of 2000 volts requires 4 voltage steps of 500 volts each, 3 pin combinations, and 3 devices per pin combination per voltage level for a maximum total of 36 devices.

Maximum # of devices = (# of pin combinations) X (# of voltage steps required) X 3 devices
3.2 Pin Combinations

The pin combinations to be used are given in Table 2. The actual number of pin combinations depends on the number of power pin groups. Power pins of the same name (VCC1, VCC2, VSS1, VSS2, etc.) may be tied together and considered one (1) power pin group if they are connected in the package or on the chip via a metal line. Same name power pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other, must be treated as a separate power pin group. All pins configured as "no connect" pins shall be considered non-supply pins and included in the pin groups stressed during ESD testing. Integrated Circuits with six (6) pins or less shall be tested using all possible pin pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function.

Table 2: Pin Combinations for Integrated Circuits

<table>
<thead>
<tr>
<th>Pin Combination</th>
<th>Connect Individually to Terminal A (Stress)</th>
<th>Connect Individually to Terminal B (Ground)</th>
<th>Floating Pins (unconnected)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>All pins one at a time, except the pin(s) connected to Terminal B</td>
<td>First power pin(s)</td>
<td>All pins except PUT and first power pin(s)</td>
</tr>
<tr>
<td>2</td>
<td>All pins one at a time, except the pin(s) connected to Terminal B</td>
<td>Second power pin(s)</td>
<td>All pins except PUT and second power pin(s)</td>
</tr>
<tr>
<td>3</td>
<td>All pins one at a time, except the pin(s) connected to Terminal B</td>
<td>Nth power pin(s)</td>
<td>All pins except PUT and Nth power pin(s)</td>
</tr>
<tr>
<td>4</td>
<td>Each Non-supply pin</td>
<td>All other Non-supply pins except PUT</td>
<td>All power pins</td>
</tr>
</tbody>
</table>

3.3 Test Temperature

Each device shall be subjected to ESD pulses at room temperature.

3.4 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3.5 Detailed Procedure

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Set the pulse voltage at 500 volts. Voltage level skipping is not allowed.

b. Connect a power pin group to terminal B. Leave all other power pins unconnected (see Table 2 / pin combination 1).

c. Connect an individual pin to terminal A. Leave all other pins unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

f. Disconnect the PUT from testing and connect the next individual pin to terminal A. Leave all other pins unconnected.

g. Repeat steps (d) through (f) until every pin not connected to terminal B is pulsed at the specified voltage.

h. Repeat steps (b) through (g) until all power pin groups have been stressed (see Table 2 / pin combinations 2 and 3). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

i. Connect one non-supply pin to terminal A and tie all other non-supply pins to terminal B. Leave all power pins unconnected (see Table 2 / pin combination 4). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

j. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

k. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

l. Disconnect the PUT from testing and connect the next non-supply pin to terminal A. Tie all non-supply pins not under test to terminal B. Leave all other pins unconnected (see Table 2 / pin combination 4).

m. Repeat steps (j) through (l) until all non-supply pins have been tested.

n. Test the next device in the sample group and repeat steps (b) through (m) until all devices in the sample group have been tested at the specified voltage level.
o. Submit the device for complete DC parametric and functional testing (final ATE verification) per the device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification, and determine whether the devices pass the failure criteria requirements specified in section 4. The functionality of “EEPROM” type devices shall be verified by programming random patterns. If a different sample group is tested for each pin combination or stress voltage level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been tested.

p. Using the next sample group, increase the pulse voltage by 500 volts and repeat steps (b) through (o). Voltage level skipping is not allowed. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group pass the failure criteria requirements specified in section 4 after exposure to a specified voltage level. If device fails at the 500 volt level, decrease the pulse voltage to 250 volts and repeat steps (b) through (o).

q. Repeat steps (b) through (p) until failure occurs or the device fails to meet the 250 volt stress voltage level.

4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5. ACCEPTANCE CRITERIA

A device passes a voltage level if all devices in the sample group stressed at that voltage level and below pass. All devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 3, the supplier shall classify the device according to the maximum withstanding voltage level.

Table 3: Integrated Circuit HBM ESD Classification Levels

<table>
<thead>
<tr>
<th>Component Classification</th>
<th>Maximum Withstand Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>H0</td>
<td>≤ 250 V</td>
</tr>
<tr>
<td>H1A</td>
<td>&gt; 250 V to ≤ 500 V</td>
</tr>
<tr>
<td>H1B</td>
<td>&gt; 500 V to ≤ 1000 V</td>
</tr>
<tr>
<td>H1C</td>
<td>&gt; 1000 V to ≤ 2000 V</td>
</tr>
<tr>
<td>H2</td>
<td>≥ 2000 V to ≤ 4000 V</td>
</tr>
<tr>
<td>H3A</td>
<td>&gt; 4000 V to ≤ 8000 V</td>
</tr>
<tr>
<td>H3B</td>
<td>&gt; 8000 V</td>
</tr>
</tbody>
</table>
Test sample of 3 devices

Submit all devices for ATE verification *

Set pulse voltage level to 500 volts

Select a pin combination for test, see Table 2

Apply positive pulses and negative pulses to pin

Next pin

All pins tested at one pin combination and one pulse voltage level

Select next pin combination for test, see Table 2 ** & *** & ****

All pins tested at all pin combinations and one pulse voltage level

Test next device

All devices tested at all pin combinations and one pulse voltage level

ATE verification * & ***

Next sample group ****

Increase pulse voltage level by 500 volts

Sample group tested at maximum withstanding voltage level

Testing completed

* For initial ATE verification, all devices shall be tested to complete DC parametric and functional requirements per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification.

** The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

*** If a different sample group is tested at each pin combination or stress voltage level, it is permitted to perform complete DC parametric and functional testing (final ATE verification) per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification, after all sample groups have completed testing.

**** It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in the sample group pass the failure criteria requirements specified in section 4 after exposure to a specified pulse voltage level.

Figure 4: Integrated Circuit HBM ESD Test Flow Diagram
<table>
<thead>
<tr>
<th>Rev #</th>
<th>Date of change</th>
<th>Brief summary listing affected sections</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>June 9, 1994</td>
<td>Initial Release</td>
</tr>
<tr>
<td>A</td>
<td>May 15, 1995</td>
<td>Added copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, i, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.</td>
</tr>
<tr>
<td>B</td>
<td>Sept. 6, 1996</td>
<td>Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.3, 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Figures 1 and 4.</td>
</tr>
<tr>
<td>C</td>
<td>Oct. 8, 1998</td>
<td>Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (d, e, j, and k); Tables 1 and 2; Figure 1. Revision to section 3.5 (d, e, j, and k) reflects a change from three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses at each stress polarity to one (1) ESD pulse with a 500 millisecond minimum delay between consecutive ESD pulses. The use of three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses is also acceptable. Revision to Table 1 reflects a ±10% tolerance applied to all loads (Lpeak for short) parameter values.</td>
</tr>
<tr>
<td>D</td>
<td>July 18, 2003</td>
<td>Revision to sections 3.5 (p &amp; q) and 5 reflect addition of classification levels for ESD testing and lower voltage step for devices failing 500V. New Table 3 added listing HBM ESD classification levels.</td>
</tr>
</tbody>
</table>