Creating Xnets for Resistor Packs in Allegro PCB Editor

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Creating Xnets in Allegro PCB Editor

Purpose
This application note describes the creation of Xnets for a resistor pack part or other similar multi-pin device.

Audience
This document is intended for Allegro PCB Editor users who want to create and use extended nets “Xnets” in Allegro PCB Editor. Specifically for Creating Xnets across a multi pin device like a resistor pack.

This module covers:

- Definition of an Xnet
- Purpose of an Xnet
- Xnets through a resistor pack
- Creating an Xnet using model assignment
- Modifying the ESpice model to create pin pairs

Definition of an Xnet
An Xnet (Extended net) is a connection of 2 nets that are electrically connected through a passive discrete component, typically a resistor. From a logical perspective they are the same. The image below shows a schematic of 2 base nets and the Xnet representing their logical path from the driver to the receiver device.
Creating Xnets in Allegro PCB Editor

Purpose of an Xnet
As mentioned above, an Xnet is the logical interconnect between a driver and a receiver through a discrete component (typically a resistor). Xnets are required in electrical constraint applications to constrain a logical net in length or time from a driver to receiver through the discrete part. Making an Xnet enables the ability to constrain a net from the driver to a receiver through a discrete component in Allegro’s Constraint Manager system.

Xnets Through a Resistor Pack
Xnets that form through a resistor pack are conceptually and procedurally the same as single resistor Xnets. The additional challenge over making traditional Xnets is that the ESpice model created for the resistor pack must be modified to create the correct pin connections to form the proper Xnets through the multiple resistors. As shown in the image below an Xnet must be made through pins 1 and 8, 2 and 7, 3 and 6, and 4 and 5.

Creating an Xnet Using Model Assignment
To create an Xnet, a SPICE based model of the discrete part must be attached to the discrete part. In Allegro, this is known as assigning a signal model. Essentially it’s a property attached to the part that references a text based SPICE model that gets embedded in the Allegro BRD database. The model assignment feature is used to assign a signal model to a part.

It is possible that the Auto Setup functionality in the Signal Model Assignment form will automatically create a model for the resistor pack. If it doesn’t, follow the steps below.

1. Open your Board file (.brd) in Allegro PCB Editor.
2. Zoom into the area of the board where the resistor is that you want to make an Xnet through.
3. Select Analyze > Model Assignment
4. If the SI Design Audit window opens either resolve the errors or select **Ignore Errors > All**. This application note does not cover all aspects of setting up a design for SI analysis.

The Signal Model Assignment window opens. This dialog box manages the signal models based on devices for the entire PCB database. The Devices tab lists models per device, the RefDesPin tab lists the models by reference designator. This dialog box also enables you to assign signal models.

5. Select the resistor pack on the Allegro canvas and the corresponding device will be selected in the Model Assignment form. Once the device is selected click the **Create Model** button.
6. The Create Device Model form opens asking what type of device (IBIS or ESpice) to create. To form an Xnet an ESpice model is required. Select OK to create an ESpice Device model.

7. The Create ESpice Device Model form opens. The value of the resistor is derived from the VALUE property on the schematic. If no value exists enter in any value; the value is only relevant for doing simulation but not for creating Xnets. Note the single pins value. This value needs to be modified to create the desired pin pairs for the Xnets.
8. Modify the single pins field to make the desired pin pairs. Specifically for this example entering the string 1 8 2 7 3 6 4 5 makes the pin pairs (1 8) (2 7) (3 6) and (4 5)

9. Change the model name if desired or leave the default. Select OK to save the model and exit the form.

The ESpice model has been created with the correct pin pairs. To view or modify the pin pairs continue on with the next section of this Application Note.

Modifying the ESpice Model to Create Pin Pairs
This section only needs to be completed if you need to modify the ESpice model that was just created or to view the ESpice model.

1. In the Signal Model Assignment form select the Edit Model button to open the ESpice model in a text editor.
2. The ESpice model is a text SPICE circuit and is opened in a text editor. Scroll to the bottom where the PinConnections section is. The PinConnections portion tells Allegro which pins are logically connected to make an Xnet. This section needs to be modified to create the correct Xnets through the resistors in the pack. Referencing the schematic at the top of this document, the pin pairs that need to be created are pins 1 and 8, 2 and 7, 3 and 6, and 4 and 5. This is done by adding the following text into the ESpice model under the pin pairs section.

```
(PinConnections
  (1 8 )
  (8 1 )
  (2 7 )
  (7 2 )
  (3 6 )
  (6 3 )
  (4 5 )
  (5 4 ) )
```

3. Once the PinConnections text has been added/changed, save the ESpice model and close the text editor.

4. Select **OK** in the Signal Model Assignment form.

The Xnets are now created across the resistors in the Resistor pack.

**Summary**

In summary, to create an Xnet in Allegro PCB editor an ESpice model must be assigned to the discrete part bisecting the 2 nets. If the discrete part is a multi-pin device such as a resistor pack the ESpice model may need to be modified to create the correct pin pairs connecting the 2 pins of the resistors in the Rpack.