Freescale Semiconductor
Application Note

Document Number: AN2910
Rev. 2, 03/2007

Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces

by *DSD Applications*
Freescale Semiconductor, Inc.
Austin, TX

The design guidelines presented in this document apply to products that leverage the DDR2 SDRAM IP core, and they are based on a compilation of internal platforms designed by Freescale Semiconductor, Inc. The purpose of these guidelines is to minimize board-related issues across multiple memory topologies while allowing maximum flexibility for the board designer.

Because numerous memory topologies and interface frequencies are possible on the DDR2 SDRAM interface, Freescale highly recommends that the system/board designer verify all design aspects (signal integrity, electrical timings, and so on) through simulation before PCB fabrication.

Contents

freescale™ semiconductor

1 Designer's Checklist

In the following checklist, some of the items are phrased as question, others as requirements. In all cases, we recommend that you consider the line item and check it off in the rightmost column of Table 1.

Table 1. DDR2 Designer's Checklist

Item	Description	Yes/No
Simulation		
1.	Have optimal termination values, signal topology, trace lengths been determined through simulation for each signal group in the memory implementation? If on-die termination is used at both the memories and the controller, no additional termination is required for the data group. Four unique groupings exist: (1). Data Group: MDQS(8:0), $\overline{\text{MDQS}}$(8:0), MDM(8:0), MDQ(63:0), MECC(7:0) (2). Address/CMD Group: MBA(2:0), MA(15:0), $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MWE}}$. (3). Control Group: $\overline{\text{MCS}}$(3:0), MCKE(3:0), MODT(3:0) (4). Clock Group: MCK(5:0) and $\overline{\text{MCK}}$(5:0) These groupings assume a full 72-bit data implementation (64-bit + 8 bit of ECC). Some products may only implement 32-bit data and may choose to have less $\overline{\text{MCS}}$ MCKE, and MODT signals. Secondly, some products support the optional MAPAR_OUT and $\overline{\text{MAPAR\_ERR}}$ for registered DIMMs. In such cases, MAPAR_OUT should be treated as part of the ADDR/CMD group and $\overline{\text{MAPAR\_ERR}}$ can be treated as an asynchronous signal.	
2.	Does the selected termination scheme meet the AC signaling parameters (voltage levels, slew rate, overshoot/undershoot) across all memory chips in the design?	
Termination Scheme It is assumed that the designer is using the mainstream termination approach as found in commodity PC motherboards. Specifically, it is assumed that on-die termination is used for the data groups and that external parallel resistors tied to VTT are used for the Address/CMD and the control groups. Consequently, differing termination techniques may also prove valid and useful. However, they are left to the designer to validate through simulation.		
3.	Is the worst case power dissipation for the termination resistors within the manufacturer's rating for the selected devices? See Section 2, "Termination Dissipation".	
4.	If resistor packs are used, have data lanes been isolated from the other DDR2 signal groups? **Note:** Because on-die termination is the preferred method for DDR2 data signals, external resistors for the data group should not be required. This item would only apply if the ODT feature is not used.	
5.	Have V_{TT} resistors been properly placed? The R_T terminators should directly tie into the V_{TT} island at the end of the memory bus.	
6.	If series damping (R_S) terminators are used (not seen as mainstream approach), were they placed close to the first memory DIMM? For discrete implementations—Placement of the series damping resistor (R_S) for the data group is left to the board designer. This trade-off is optimal signal integrity for both reads/writes (R_S in middle) versus ease of layout routing (R_S placed closer to memory devices).	

Table 1. DDR2 Designer's Checklist (continued)

Item	Description	Yes/No
7.	For address and command signals, the Micron compensation cap scheme is another optional termination method for improving eye apertures for a heavily loaded system (> 18 memory chips). For details on this termination scheme refer to *DDR533 Memory Design for Two-DIMM Unbuffered Systems,* located on Micron's web site. For lightly and medium loaded memory subsystems (4–18 chips), the compensation cap method is not as beneficial. If used, are the C_{COMP} capacitors placed within 0.5 inch of the first memory bank?	
8.	Is the differential terminator present on the clock lines for discrete memory populations? (DIMM modules contain this terminator.) Nominal range => 100-120 Ω.	
9.	Recommend that an optional 5pF cap be placed across each clock diff pair. If DIMM modules are used, the cap should be placed as closely as possible to the DIMM connector. If discrete devices are used, the cap should be placed as closely as possible to the discrete devices.	
10.	Recommendation—Place 0-Ω resistors on the DDR2 clock lines (near the driver). Such flexibility allows the clock lengths to be extended (if needed) during the prototyping phase.	
V_{TT} Related Items		
11.	Has the worst case current for the V_{TT} plane been calculated based on the design termination scheme? See Section 2, "Termination Dissipation".	
12.	Can the V_{TT} regulator support the steady state and transient current needs of the design?	
13.	Has the V_{TT} island been properly decoupled with high frequency decoupling? At least 1 low ESL cap, or 2 standard decoupling caps for each 4-pack resistor network (or every 4 discrete resistors) should be used. In addition, at least one 4.7-µF cap should be at each end of the V_{TT} island. **Note:** This recommendation is based on a top-layer V_{TT} surface island (lower inductance). If an internal split is used, more capacitors may be needed to handle the transient current demands.	
14.	Has the V_{TT} island been properly decoupled with bulk decoupling? At least 1 bulk cap (100–220 µF) capacitor should be at each end of the island.	
15.	Has the V_{TT} island been placed at the end of the memory channel and as closely as possible to the last memory bank? Is the V_{TT} regulator placed in close proximity to the island?	
16.	Is a wide surface trace (~150 mils) used for the V_{TT} island trace?	
17.	If a sense pin is present on the V_{TT} regulator, is it attached in the middle of the island?	
V_{REF}		
18.	Is V_{REF} routed with a wide trace? (Minimum of 20–25 mil recommended.)	
19.	Is V_{REF} isolated from noisy aggressors? In addition, maintain at least a 20–25 mil clearance from V_{REF} to other traces. If possible, isolate V_{REF} with adjacent ground traces.	
20.	Is V_{REF} properly decoupled? Specifically, decouple the source and each destination pin with 0.1uf caps.	
21.	Does the V_{REF} source track variations in VDDQ, temperature, and noise as required by the JEDEC specification?	
22.	Does the V_{REF} source supply the minimal current required by the system (memories + processor)?	
23.	If a resistor divider network is used to generate V_{REF}, are both resistors the same value and 1% tolerance?	
Routing		

Table 1. DDR2 Designer's Checklist (continued)

Item	Description	Yes/No
24.	Suggest routing order within the DDR2 interface: 1) Data, 2) Address/Command, 3) Control, 4) Clocks, and 5) Power This order allows the clocks to be tuned easily to the other signal groups. It also assumes an open critical layer on which clocks are freely routed.	
25.	Global items— • Do not route any DDR2 signals overs splits or voids. • Traces routed near the edge of a reference plane should maintain at least 30–40 mil gap to the edge of the reference plane. • Allow no more than 1/2 of a trace width to be routed over via antipad.	
26.	When routing the data lanes, route the outermost (that is, longest lane first) because this determines the amount of trace length to add on the inner data lanes.	
27.	Are the clock pair assignments optimized to allow break-out of all pairs on a single critical layer?	
28.	The DDR2 data bus consists of 9 data byte lanes (assuming ECC is used). All signals within a given byte lane should be routed on the same critical layer with the same via count. Note: Some product implementations may only implement a 32-bit wide interface. Byte Lane 0—MDQ(7:0), MDM(0), MDQS(0), $\overline{\text{MDQS}}$(0) Byte Lane 1—MDQ(15:8), MDM(1), MDQS(1), $\overline{\text{MDQS}}$(1) Byte Lane 2—MDQ(23:16), MDM(2), MDQS(2), $\overline{\text{MDQS}}$(2) Byte Lane 3—MDQ(31:24), MDM(3), MDQS(3), $\overline{\text{MDQS}}$(3) Byte Lane 4—MDQ(39:32), MDM(4), MDQS(4), $\overline{\text{MDQS}}$(4) Byte Lane 5—MDQ(47:40), MDM(5), MDQS(5), $\overline{\text{MDQS}}$(5) Byte Lane 6—MDQ(55:48), MDM(6), MDQS(6), $\overline{\text{MDQS}}$(6) Byte Lane 7—MDQ(63:56), MDM(7), MDQS(7), $\overline{\text{MDQS}}$(7) Byte Lane 8—MECC(7:0), MDM(8), MDQS(8), $\overline{\text{MDQS}}$(8) To facilitate fan-out of the DDR2 data lanes (if needed), alternate adjacent data lanes onto different critical layers? See Figure 1 and Figure 2. **Note:** If the device supports ECC, Freescale highly recommends that the user implement ECC on the initial hardware prototypes.	
29.	DDR2 data group—Impedance range and spacing • Single-ended target Impedance = 50–60 Ω range (MDQ, $\overline{\text{MDM}}$) • Differential target impedance = 100–120 Ω range (MDQS, $\overline{\text{MDQS}}$) Note: Some product implementations may support only the single-ended version of the strobe. • Referenced to a solid ground plane, thereby providing a low-impedance path for return currents. • Trace space to other non-DDR2 data groups = 25 mil. • Trace space requirements within the DDR2 data group = 10 mils (reducing to 7 mils inside the DIMM area). **Note:** Based on a trace width of 5 mil.	
30.	Across all DDR2 data lanes, are all the data lanes matched to within 0.5 inch?	
31.	Is each data lane properly trace matched to within 20 mils of its respective differential data strobe? (Assumes highest frequency operation.)	
32.	When adding trace lengths to any of the DDR2 signal groups, ensure that there is at least 25 mils between serpentine loops that are in parallel.	

Table 1. DDR2 Designer's Checklist (continued)

Item	Description	Yes/No
33.	MDQS/$\overline{\text{MDQS}}$ differential strobe routing Note: Some product implementations may support only the single-ended version of the strobe. • Match all segment lengths between differential pairs along the entire length of the pair. Trace match the MDQS/ $\overline{\text{MDQS}}$ pair to be within 10 mils. • Maintain constant line impedance along the routing path by maintaining the required line width and trace separation for the given stackup. • Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips. • Differential Impedance = 100–120 (50–60 Ω single ended with proper spacing) • Do not divide the two halves of the diff pair between layers. Route MDQS/$\overline{\text{MDQS}}$ pair on the same critical layer as its associated data lane.	
34.	DDR2 address/command group—Impedance range and spacing • Single-Ended Target Impedance = 50–60 Ω range • Match all traces to within 100 mils • Referenced to a contiguous 1.8-V power reference (DIMM implementations currently do this) • Referenced to a contiguous 1.8-V power reference or ground plane (discrete implementations) • Trace space to other non-DDR2 address/cmd signals = 25 mil. • Trace space requirements within the DDR2 address/cmd group = 10 mils (reducing to 7 mils inside the DIMM area). **Note:** Based on a trace width of 5 mil.	
35.	DDR2 control group—Impedance range and spacing • Single-Ended Target Impedance = 50–60 Ω range • Match all traces to within 100 mils • Referenced to a contiguous 1.8-V power reference (DIMM implementations currently do this) • Referenced to a contiguous 1.8-V power reference or ground plane (discrete implementations) • Trace space to other non-DDR2 control groups = 25 mil. • Trace space requirements within the DDR2 control group = 10 mils (reducing to 7 mils inside the DIMM area). **Note:** Based on a trace width of 5 mil.	
36.	Are the DDR2 signal groups tuned to the clock reference? Because this is loading and topology dependent, the variance around the clock should be determined by simulation. Secondly, in multi-bank systems, are the address and command signals loaded more heavily than the control signals (CS, ODT, CKE)? Specifically: • Are the setup/hold optimized for the addr/cmd group? • Are the steup/hold optimized for the control group (CS, ODT, CKE)? • Is the write data delay window met (t_{DQSS})? This is the relationship between the data strobes and clocks as specified by the JEDEC DDR2 specification.	
37.	Are the DDR2 differential clocks properly routed? • Match all segment lengths between differential pairs along the entire length of the pair. Trace match the MCK/ $\overline{\text{MCK}}$ pair to be within 10 mils. • Maintain constant line impedance along the routing path by maintaining the required line width and trace separation for the given stackup. • Avoid routing differential pairs adjacent to noisy signals lines or high speed switching devices such as clock chips. • Differential Impedance = 100–120 (50–60 Ω single ended with proper spacing) • Do not divide the two halves of the diff pair between layers. Route MCK/$\overline{\text{MCK}}$ pair on the same critical layer.	
38.	Are all clock pairs routed on the same critical layer (one referenced to a solid ground plane)?	
39.	Are all clock pairs properly trace matched to within 25 mils of each other?	

Table 1. DDR2 Designer's Checklist (continued)

Item	Description	Yes/No
40.	The space from one differential pair to any other trace (this includes other differential pairs) should be at least 25 mils.	
41.	If unbuffered DIMM modules are used, are all three required clock pairs per DIMM slot connected?	
42.	If the optional 0-Ω resistors are used (as noted in item 10), use ground stitching vias near the resistors.	
MODT/MDIC Related Items		
43.	Are the MODT signals connected correctly? MODT(0), $\overline{\text{MCS}}$(0), MCKE(0) should all go to the same physical memory bank. MODT(1), $\overline{\text{MCS}}$(1), MCKE(1) should all go to the same physical memory bank. MODT(2), $\overline{\text{MCS}}$(2), MCKE(2) should all go to the same physical memory bank. MODT(3), $\overline{\text{MCS}}$(3), MCKE(3) should all go to the same physical memory bank.	
44.	Is MDIC0 connected to ground via an 18.2-Ω precision 1% resistor? Is MDIC1 connected to DDR power via an 18.2-Ω precision 1% resistor?	
Miscellaneous Items		
45.	Keep the memory channel (area between controller and the memory) free of noisy and high frequency components (ideal case is to place only memory terminators and decoupling within this area).	
46.	Are the power-on reset config pins properly set for the correct DDR type? **Note:** Not all Freescale products support external power-on reset configuration pins for selecting the DDR type. Therefore, this item does not apply to all Freescale products.	
Registered DIMM Topologies (All items above still apply)		
47.	For memory implementations that use registered DIMM modules, the board designer should attach a reset signal to the DIMM sockets. This reset signal should be derived from a 'power good' monitor status circuit.	
48.	Though registered DIMMs require only a single clock per bank, all DDR2 clock pairs at the DIMM connector should be attached (analogous to unbuffered DIMMs) so the design can also support unbuffered DIMMs with minimal changes.	
49.	If the controller supports the optional MAPAR_OUT and $\overline{\text{MAPAR\_ERR}}$ signals, ensure that they are hooked up as follows: MAPAR_OUT (from the controller) => PAR_IN (at the RDIMM). ERR_OUT (from the RDIMM) => $\overline{\text{MAPAR\_ERR}}$ (at the controller).	
50.	$\overline{\text{MAPAR\_ERR}}$ is an open drain output from registered DIMMs. Ensure that a 4.7K pull-up to 1.8 V is present on this signal.	
Discrete Memory Topologies (All items above still apply with exception of registered DIMM items)		
51.	Construct the signal routing topologies for the groups like those found on unbuffered DIMM modules (that is, proven JEDEC topologies).	
52.	When placing components, optimize placement of the discretes to favor the data bus (analogous to DIMM topologies). Optional: Pin-swap within a given byte lane to optimize the data bus routes further. **Caution:** Do not swap individual data bits across different byte lanes.	

Table 1. DDR2 Designer's Checklist (continued)

Item	Description	Yes/No
53.	If a single bank of x16 devices is used, let the DDR2 clocks be point-to-point. Place the series damping resistor (R_S) close to the source and the differential terminator (R_{DIFF}) at the input pins of the discretes. If more than 5 discretes are used, construct the clocks like those on unbuffered DIMM modules. Alternatively, place an external PLL between the controller and the memory to generate the additional clocks.	
54.	If multiple physical banks are needed, double stack (top and bottom) the banks to prevent lengthy and undesirable address/cmd topologies.	
55.	Properly decouple the DDR2 chips per manufacturer recommendations. Typically, five low ESL capacitors per device are sufficient. For further information, see article entitled *Decoupling Capacitor Calculation for a DDR Memory Channel,* located on Micron's web site.	
56.	To support expandability into larger devices, ensure that extra NC pins (future address pins) are connected.	
57.	Ensure access/test points are available for signal integrity probing. This is especially critical if using blind and buried vias within the memory channel. If through-hole vias are used under the BGA devices, then generally these sites can be used for probing.	

2 Termination Dissipation

Sink and source currents flow through the parallel R_T resistors on the address and control groups. The worst case power dissipation for these resistors is as follows:

$$\text{Power} = I^2 * R_T = (18.6\text{ mA})^2 * (47\ \Omega) = 16.3\text{ mW}.$$

Small compact 4-pin resistor packages (16 mm × 32 mm) that provide dissipation up to 1/16 watt (62.5 mW) are ideal. See Section 4, "VTT Voltage Rail" for assumptions made for current calculations.

3 VREF

The current requirements for V_{REF} are relatively small, at less than 3 mA. This reference provides a DC bias of 0.9V ($V_{DD}/2$) for the differential receivers at both the controller interface and the DDR devices. Noise or deviation in the V_{REF} voltage can lead to potential timing errors, unwanted jitter, and erratic behavior on the memory bus. To avoid these problems, V_{REF} noise must be kept within the JEDEC specification. As such, V_{REF} and the V_{TT} cannot be the same plane because of the DRAM V_{REF} buffer sensitivity to the termination plane noise. However, both V_{REF} and V_{TT} must share a common source supply to ensure that both are derived from the same voltage plane. Proper decoupling at each V_{REF} pin (at the controller, at each DIMM/discrete, and at the V_{REF} source) along with the adhering to the simple layout considerations enumerated in the checklist prevents potential problems.

Numerous off-the-shelf power solutions can provide both the V_{REF} and V_{TT} from a common circuit. Regardless of the generation technique, V_{REF} must track variations in V_{DDQ} over voltage, temperature, and noise margins as required by the JEDEC specifications.

4 V_{TT} Voltage Rail

For a given topology, the worst case V_{TT} current should be derived. Assuming the use of a typical R_T parallel termination resistor and the worst case parameters give in Table 4-2, sink and source currents can be calculated.

Table 4-2. Worst Case Parameters for V_{TT} Current Calculation

Parameter	Values	Comment
V_{DDQ}(max)	1.9 V	From JEDEC spec
V_{TT}(max)	0.958 V	From JEDEC spec
V_{TT}(min)	0.842 V	From JEDEC spec
R_{DRVR}	10 Ω	Nominally, full strength is ~ 18 Ωs
R_T	47 Ω	Can vary. Typically 25-47Ωs.
V_{OL}	0 V	Assumes driver reaches 0 V in the low state.

The driver would source (V_{TT} plane would sink) the following based on this termination scheme:

$$(V_{DD\_max} - V_{TT\_min})/(R_T + R_{DRVR}) = (1.9\ V - 0.842\ V)/(47 + 10) = 18.6\ mA$$

The driver would sink (V_{TT} plane would source) the following based on this termination scheme:

$$(V_{TT\_max} - V_{OL} / (R_T + R_S + R_{DRVR}) = (0.958\ V - 0\ V)/(47 + 10) = 16.8\ mA$$

A bus with balanced number of high and low signals places no real demand on the V_{TT} supply. However, a bus with all DDR address/command/control signals low (~ 28 signals) causes a transient current demand of approximately 500 mA on the V_{TT} rail. The V_{TT} regulator must provide a relatively tight voltage regulation of the rail per the JEDEC specification. Besides a tight tolerance, the regulator must also allow V_{TT} along with V_{REF} (if driven from a common IC), to track variations in V_{DDQ} over voltage, temperature, and noise margins.

5 Layout Guidelines for the Signal Groups

To help ensure that the DDR interface is properly optimized, Freescale recommends the following sequence for routing the DDR memory channel:

1. Route data
2. Route address/command
3. Route control
4. Route clocks
5. Route feedback

The data group is listed before the command, address, and control group because it operates at twice the clock speed and its signal integrity is of higher concern. In addition, the data group constitutes the largest portion of the memory bus and consists of most of the trace matching requirements, those of the data lanes. The address/command, control, and data groups all have a relationship to the routed clock. Therefore, the effective clock lengths used in the system must satisfy multiple relationships. The designer should perform simulation and construct system timing budgets to ensure that these relationships are properly satisfied.

5.1 Data—MDQ[0:63], MDQS[0:8], MDM[0:8], MECC[0:7]

The data signals of the DDR interface are source-synchronous signals by which memory and the controller capture the data using the data strobe rather than the clock itself. When transferring data, both edges of the strobe are used to achieve the 2x data rate.

An associated data strobe (DQS and $\overline{\text{DQS}}$) and data mask (DM) comprise each data byte lane. This 11-bit signal lane relationship is crucial for routing. Table 5-3 depicts this relationship. When length matching, the critical item is the variance of the signal lengths within a given byte lane to its strobe. Length matching across all bytes lanes is also important and must meet the t_{DQSS} parameter as specified by JEDEC. This is also commonly referred to as the write data delay window. Typically, this timing is considerably more relaxed than the timing of the individual byte lanes themselves.

Table 5-3. Byte Lane to Data Strobe and Data Mask Mapping

Data	Data Strobe	Data Mask	Lane Number
MDQ[0:7]	MDQS0, $\overline{\text{MDQS0}}$	MDM0	Lane 0
MDQ[8:15]	MDQS1, $\overline{\text{MDQS1}}$	MDM1	Lane 1
MDQ[16:23]	MDQS2, $\overline{\text{MDQS2}}$	MDM2	Lane 2
MDQ[24:31]	MDQS3, $\overline{\text{MDQS3}}$	MDM3	Lane 3
MDQ[32:39]	MDQS4, $\overline{\text{MDQS4}}$	MDM4	Lane 4
MDQ[40:47]	MDQS5, $\overline{\text{MDQS5}}$	MDM5	Lane 5
MDQ[48:55]	MDQS6, $\overline{\text{MDQS6}}$	MDM6	Lane 6
MDQ[56:63]	MDQS7, $\overline{\text{MDQS7}}$	MDM7	Lane 7
MECC[0:7]	MDQS8, $\overline{\text{MDQS8}}$	MDM8	Lane 8

NOTE

When routing, each row (that is the 11-bit signal group) must be treated as a trace-matched group.

5.2 Layout Recommendations

Freescale strongly recommends routing each data lane adjacent to a solid ground reference for the entire route to provide the lowest inductance for the return currents, assisting the overall signal integrity of the data interface. This concern is especially critical in designs that target the top-end interface speed because the data switches at 2x the applied clock. When the byte lanes are routed, signals within a byte lane should be routed on the same critical layer as they traverse the PCB motherboard to the memories. This consideration helps minimize the number of vias per trace and provides uniform signal characteristics for each signal within the data group.

To facilitate ease of break-out from the controller perspective, and to keep the signals within the byte group together, the board designer should alternate the byte lanes on different critical layers, (see Figure 1 and Figure 2).

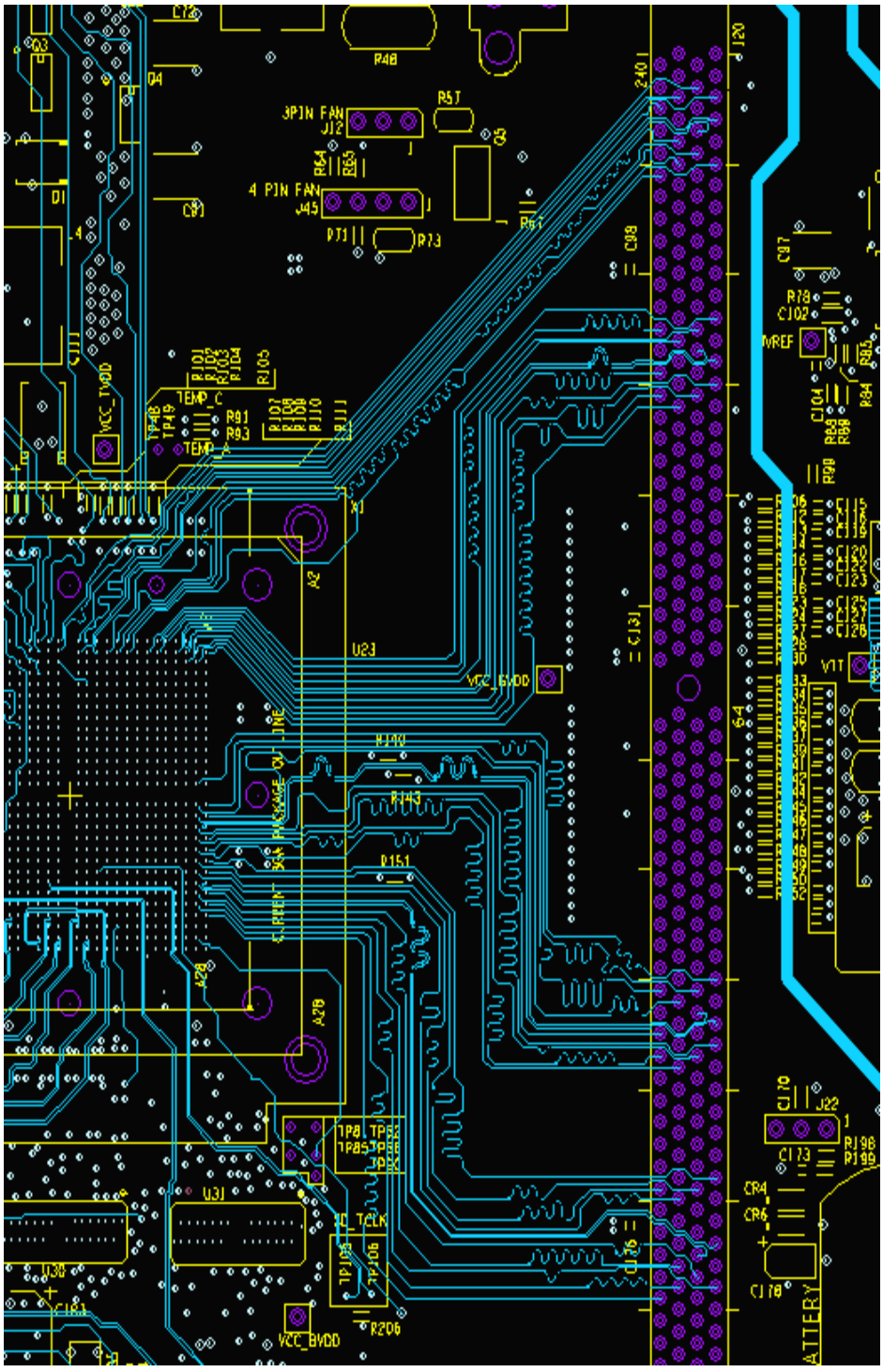

Figure 1. Alternating Data Byte Lanes on Different Critical Layers—Part 1

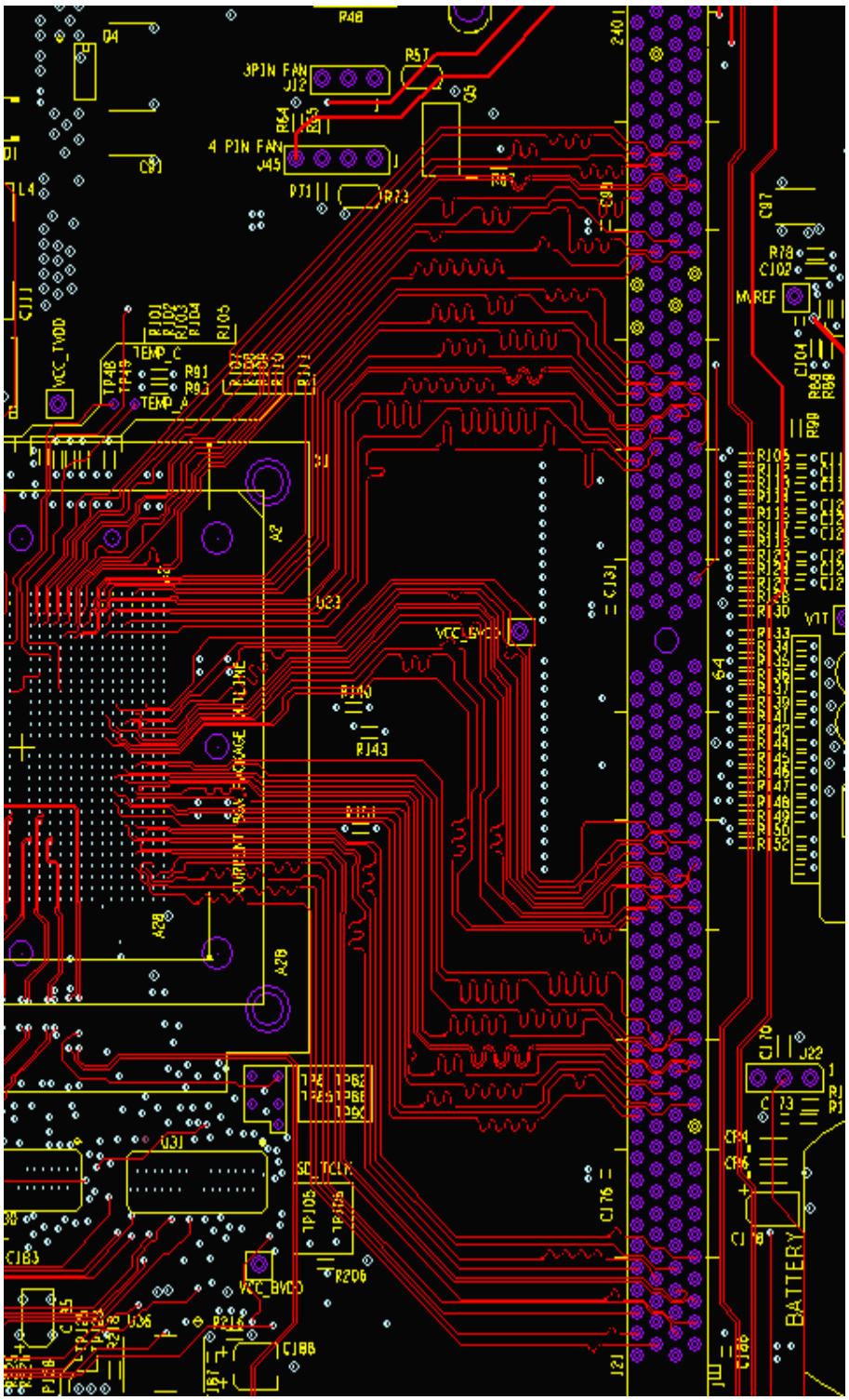

Figure 2. Alternating Data Byte Lanes on Different Critical Layers—Part 2

6 Simulation

This application note provides general hardware and layout considerations for hardware engineers implementing a DDR2 memory subsystem.The rules and recommendations in this document can serve as an initial baseline for board designers to begin their specific implementations. Numerous memory topologies and interface frequencies are possible from the DDR2 interface, so Freescale highly recommends that the board designer verify that all aspects (signal integrity, electrical timings, and so on) are addressed through simulation before board fabrication.

In tandem with memory vendors, Freescale provides IBIS models for simulation. The board designer can realize a key advantage in the form of extra noise and timing margins by taking the following actions:

- Optimizing the clock to signal group relationships to maximize setup and hold times.
- Optimizing termination values. During board simulation, verify that all aspects of the signal eye are satisfied, which includes at a minimum the following:
  - A sufficient signal eye opening meeting both timing and AC input voltage levels
  - Vswing max not exceeded (or alternatively max overshoot/max undershoot)
  - Signal slew rate within specifications

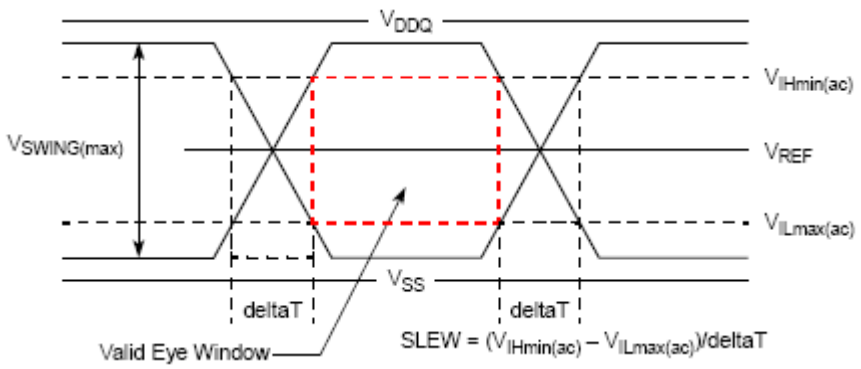

Figure 3. SSTL Signal Waveform

7 Further Reading

- DDR2 chapter of the *MPC8548 PowerQUICC™ III Integrated Communications Processor Reference Manual*
- Micron web site: http://www.micron.com. Lots of good application notes and DDR2 publications. Examples include:
  - *DDR2 Package Sizes and Layout Basics*
  - *DDR SDRAM Simulation Process*
  - *Calculating Memory System Power for DDR2 SDRAM*
  - *DDR533 Memory Design for Two-DIMM Unbuffered Systems*
  - *Decoupling Capacitor Calculation for a DDR Memory Channel*

- JEDEC web site: http://www.jedec.com
  - DDR2 SDRAM Registered DIMM Specification
  - DDR2 SDRAM Unbuffered DIMM Specification
  - DDR2 SDRAM Specification Release 2
  - SSTL18 Specification

8 Revision History

Table 4 provides a revision history for this application note.

Table 4. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	4/2007	• Incorporated Termination, VREF, VTT sections. • Updated data byte lane pictures. • Incorporated MAPAR_OUT and MAPAR_ERR to the checklist.
1	6/2006	Table 1, Item 40: Corrected resistor value to a standard 1% value
0	10/2005	Initial release.

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:
www.freescale.com

email:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: AN2910
Rev. 2
03/2007

freescale™
semiconductor