DDR2 Application Note

ODT(On Die Termination) Control

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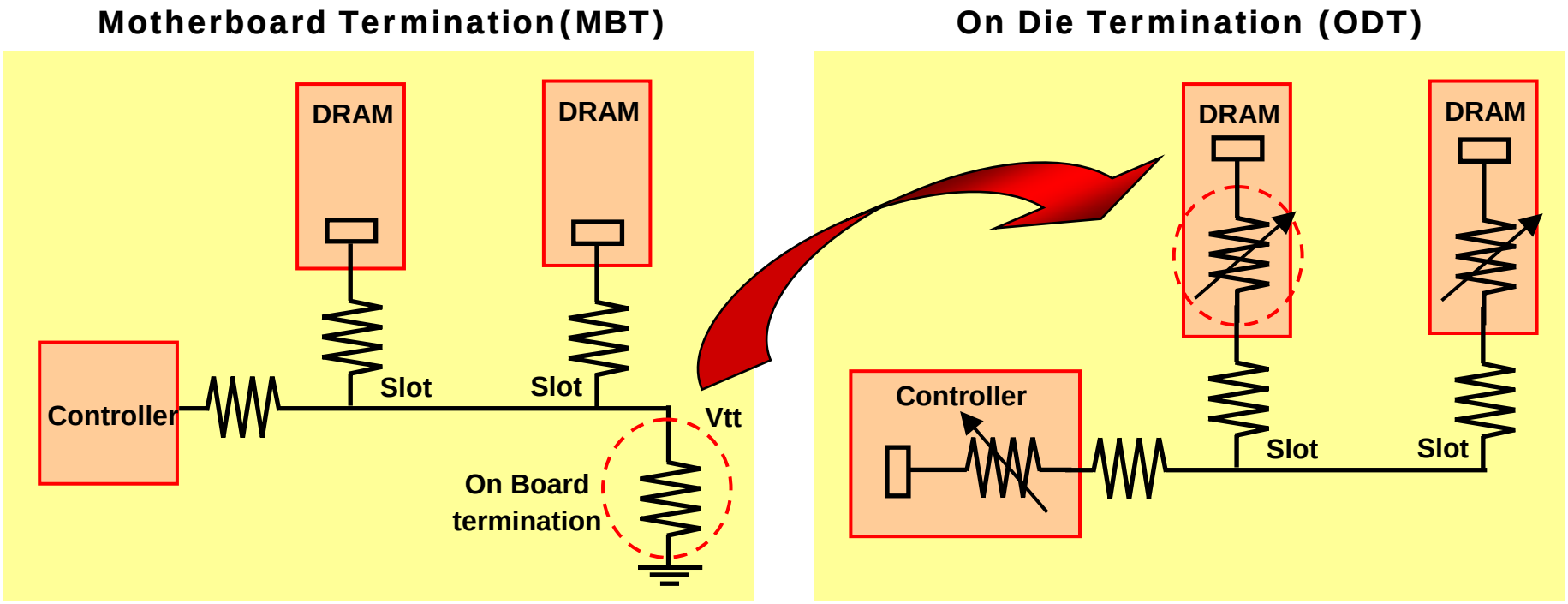
Product Planning & Application Engineering Team

MEMORY DIVISION

SAMSUNG ELECTRONICS Co., LTD

DDR2 ODT (On Die Termination)

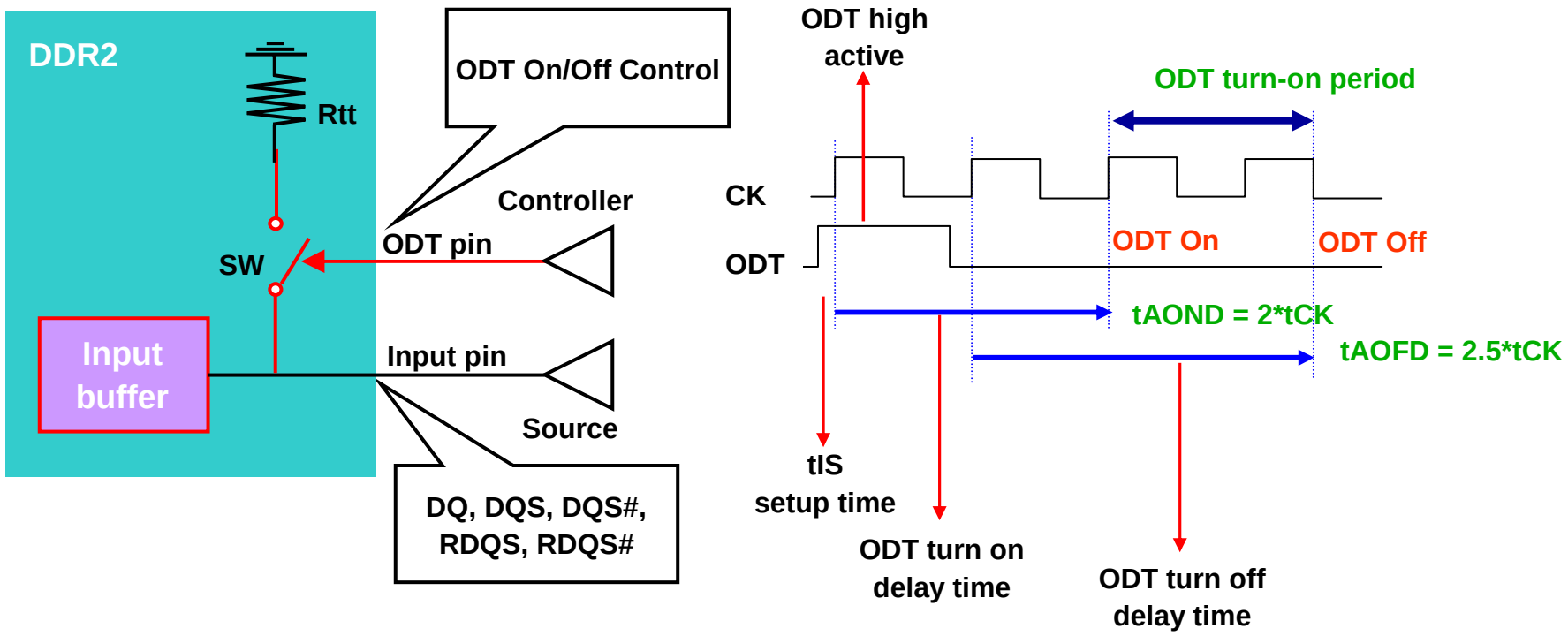
- On board termination resistance is integrated inside of DRAM



On Die Termination On / Off Control

- ODT turn on / off is controlled by ODT pin
- One ODT control pin per DRAM : Turn-on or Turn-off control
- Two ODT control pin per DIMM to support rank by rank control

But in most application, one ODT pin per slot is being used

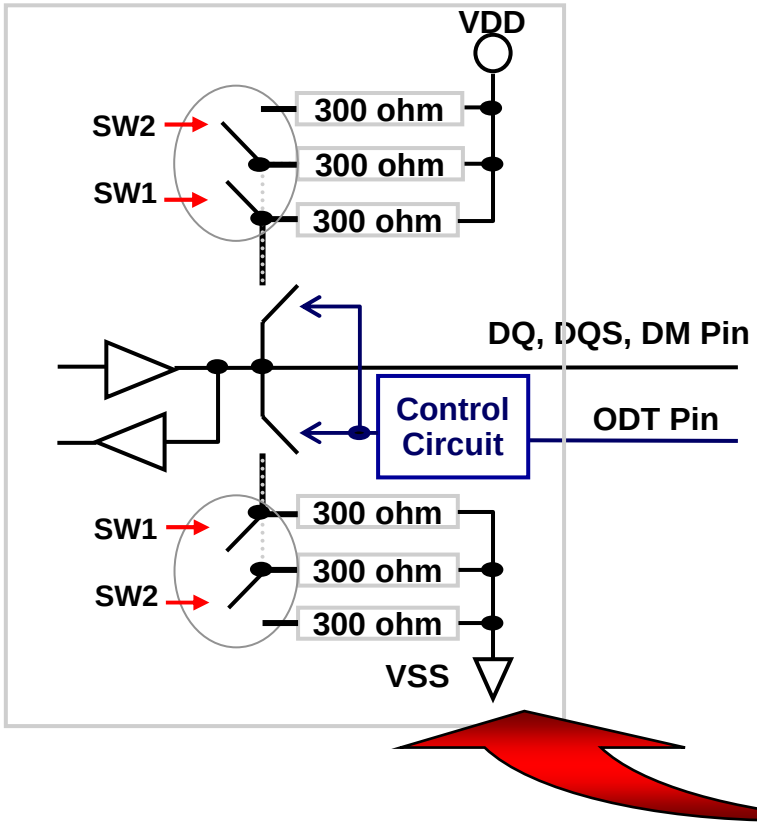


On Die Termination Value Selection

Application Note

- ODT value should be determined during power-up by EMRS

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0
	Previous Cycle	Current Cycle								
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code		



BA1	BA0	MRS Mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3) : Reserved

Address Field

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OCD program			Rtt	Additive latency			Rtt	D.S	DLL

EMRS(1)

A6	A2	Rtt (Nominal)	
0	0	ODT Disabled	
0	1	75 ohm	SW1 on
1	0	150 ohm	ODT on
1	1	50 ohm	SW2 on

Test Condition for ODT Verification

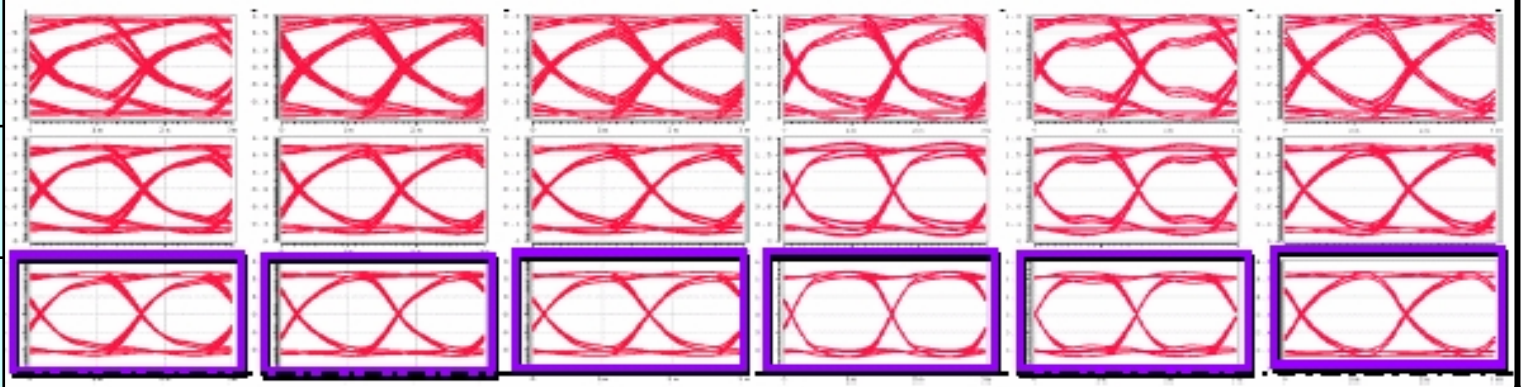
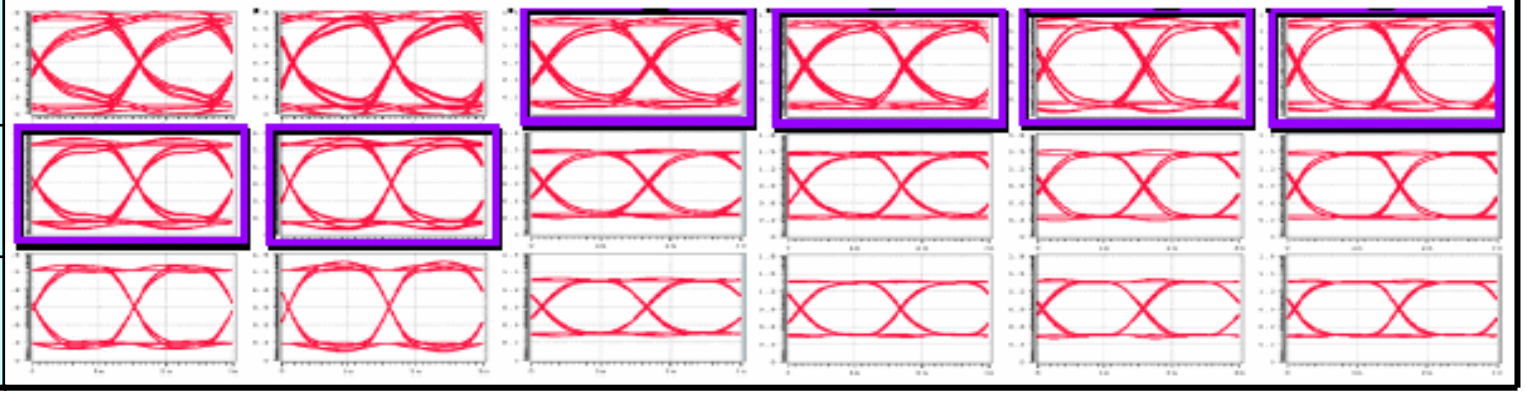
❑ Capacitance Specification for DDR2-667 & 800

Parameter	DDR2-667/DDR2-800		UNIT
	MIN	MAX	
Input capacitance CK, /CK	1.0	2.0	pF
Input capacitance Delta, CK, /CK	-	0.25	pF
Input capacitance C/A	1.0	2.0	pF
Input capacitance Delta, C/A	-	0.25	pF
Input capacitance DQ/DM/DQS	2.5	3.5	pF
Input capacitance Delta, DQ/DM/DQS	-	0.5	pF

ODT Case Study @DDR2-667 Writes

Application Note

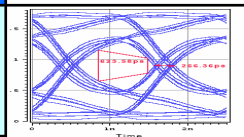
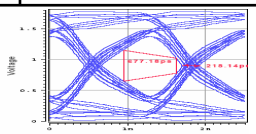
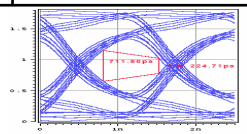
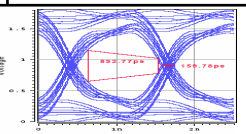
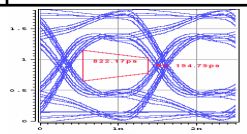
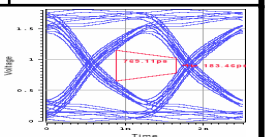
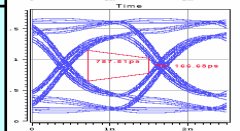
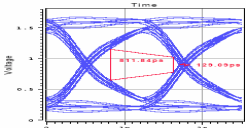
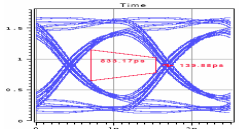
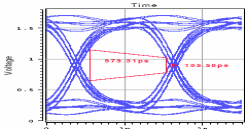
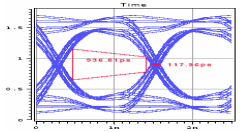
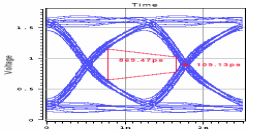
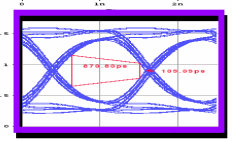
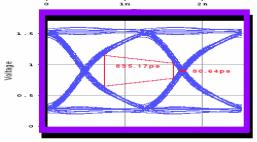
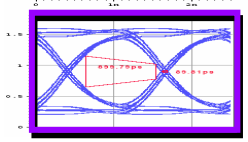
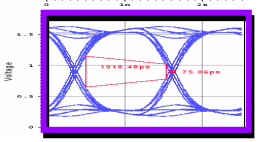
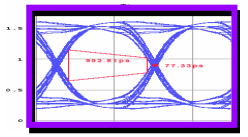
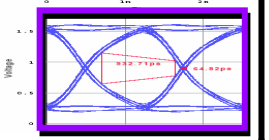
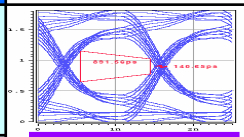
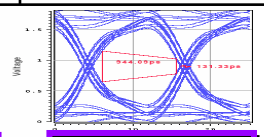
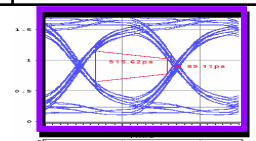
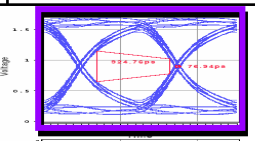
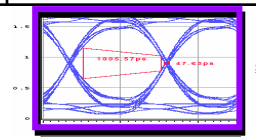
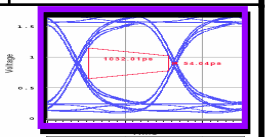
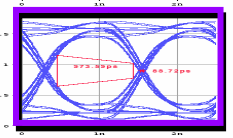
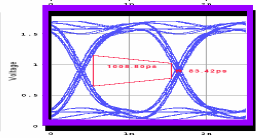
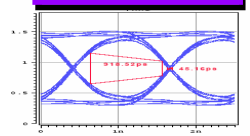
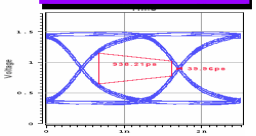
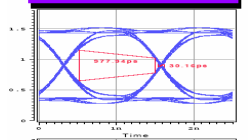
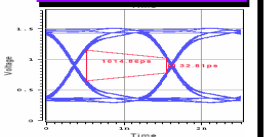
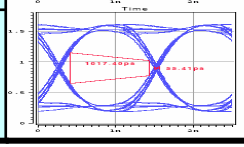
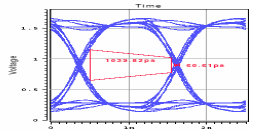
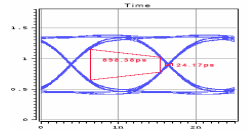
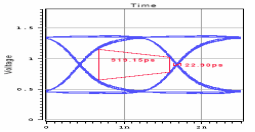
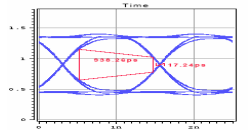
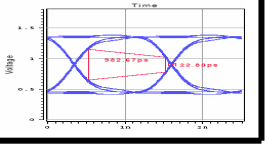
- For two slot population, 50ohm seems to be better than 75ohm in term of signal integrity
- For one slot population, even 150ohm seems O.K.

ODT value	2R 2R	2R 2R	2R 1R	2R 1R	1R 2R	1R 2R
150 ohm						
75 ohm						
50 ohm						
ODT value	**1R 1R**	**1R 1R**	**2R X**	**X 2R**	**1R X**	**X 1R**
150 ohm						
75 ohm						
50 ohm						

ODT Case Study @DDR2-800 Writes

Application Note

- For two slot population, 50ohm seems to be better than 75ohm in term of signal integrity
- For one slot population, even 150ohm seems O.K.

ODT value	2R 2R	2R 2R	2R 1R	2R 1R	1R 2R	1R 2R
150 ohm						
75 ohm						
50 ohm						
ODT value	**1R 1R**	**1R 1R**	**2R X**	**X 2R**	**1R X**	**X 1R**
150 ohm						
75 ohm						
50 ohm						

Recommended ODT Control - Writes

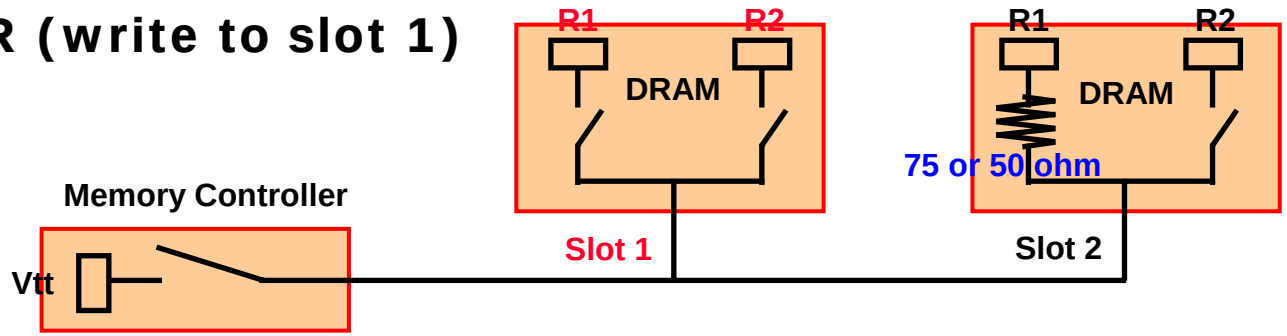
Application Note

❑ Termination Matrix for Writes to DRAM

Configuration	Write To	Target DQ ODT Resistance RTT				
		Controller	Module in slot 1		Module in slot 2	
			Rank 1	Rank 2	Rank 1	Rank 2
2R 2R	slot 1	Infinite	Infinite	Infinite	75 or 50 ohm	Infinite
	slot 2	Infinite	75 or 50 ohm	Infinite	Infinite	Infinite
2R 1R	slot 1	Infinite	Infinite	Infinite	75 or 50 ohm	Unpopulated
	slot 2	Infinite	75 or 50 ohm	Infinite	Infinite	Unpopulated
1R 2R	slot 1	Infinite	Infinite	Unpopulated	75 or 50 ohm	Infinite
	slot 2	Infinite	75 or 50 ohm	Unpopulated	Infinite	Infinite
1R 1R	slot 1	Infinite	Infinite	Unpopulated	75 or 50 ohm	Unpopulated
	slot 2	Infinite	75 or 50 ohm	Unpopulated	Infinite	Unpopulated
2R Empty	slot 1	Infinite	150 ohm	Infinite	Unpopulated	Unpopulated
Empty 2R	slot 2	Infinite	Unpopulated	Unpopulated	150 ohm	Infinite
1R Empty	slot 1	Infinite	150 ohm	Unpopulated	Unpopulated	Unpopulated
Empty 1R	slot 2	Infinite	Unpopulated	Unpopulated	150 ohm	Unpopulated

❑ ODT on a controller always turned-off

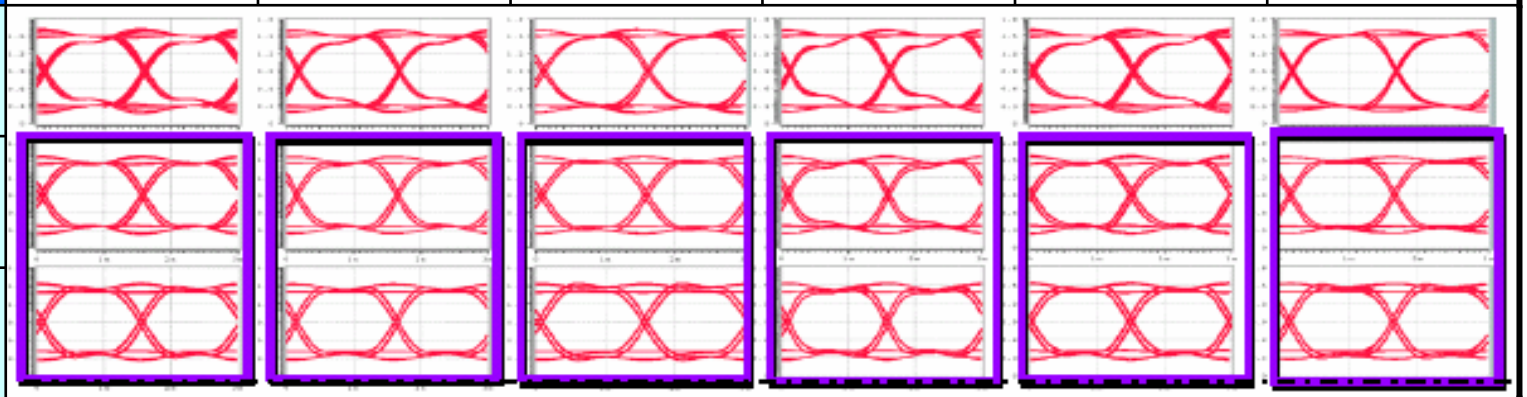
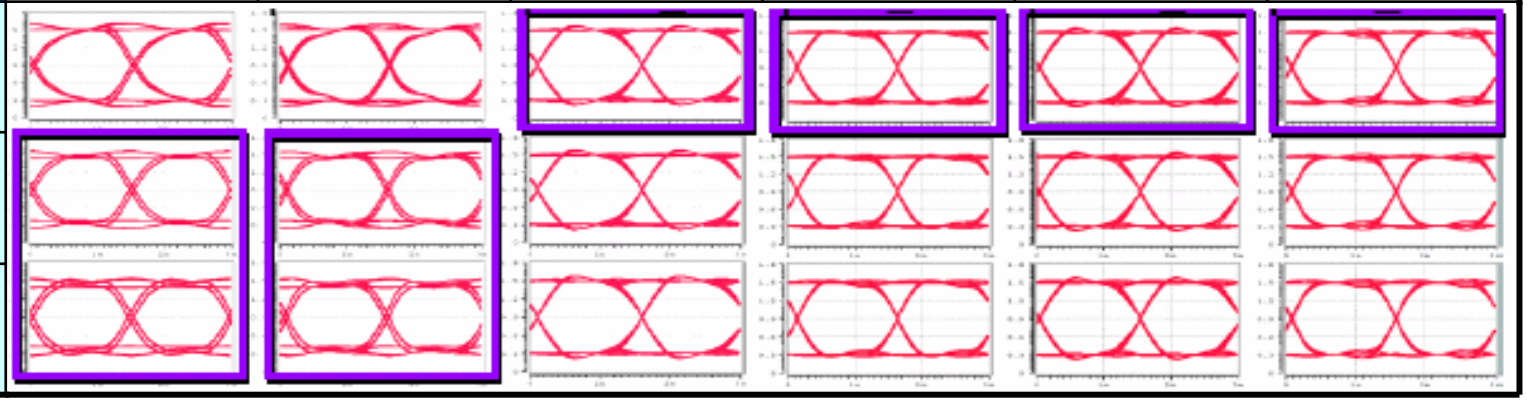
❑ Example : 2R 2R (write to slot 1)



ODT Case Study @DDR2-667 Reads

Application Note

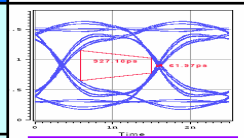
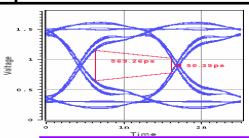
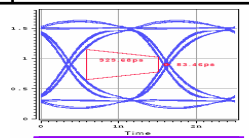
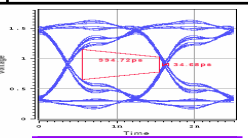
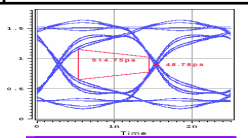
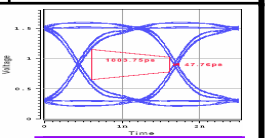
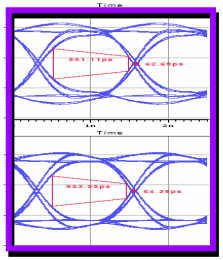
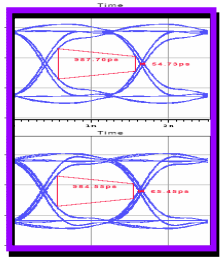
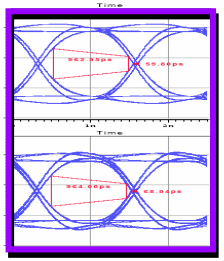
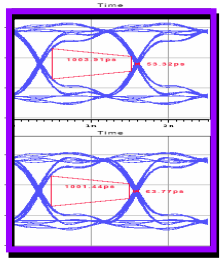
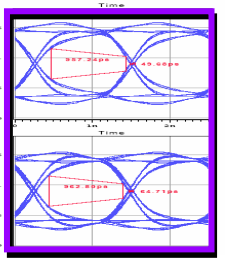
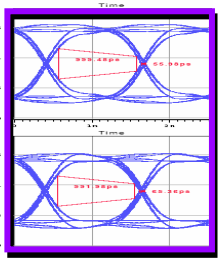
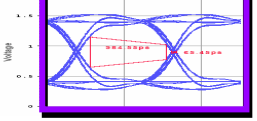
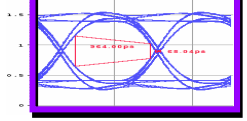
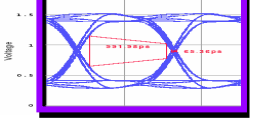
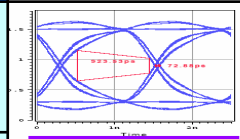
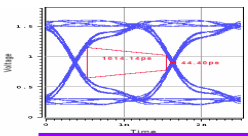
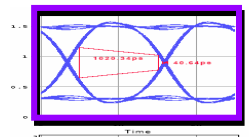
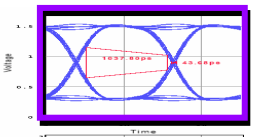
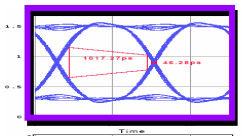
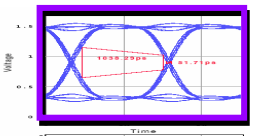
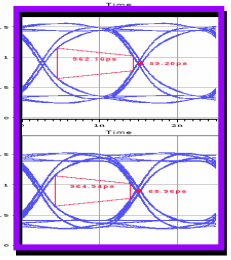
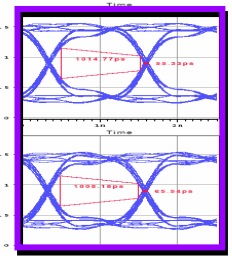
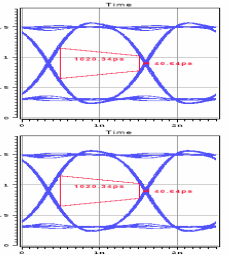
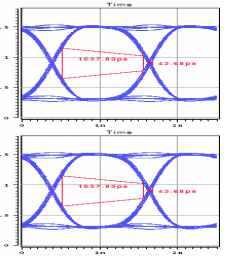
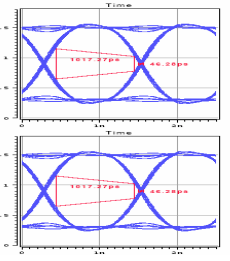
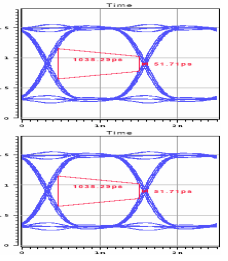
- For two slot population, either 75ohm or 50ohm could be O.K.
  → 50ohm does not help on reads that much
- For one slot population, even 150ohm seems O.K.

ODT value	2R 2R	2R 2R	2R 1R	2R 1R	1R 2R	1R 2R
150 ohm						
75 ohm						
50 ohm						
ODT value	**1R 1R**	**1R 1R**	**2R X**	**X 2R**	**1R X**	**X 1R**
150 ohm						
75 ohm						
50 ohm						

ODT Case Study @DDR2-800 Reads

Application Note

- For two slot population, either 75ohm or 50ohm could be O.K.
  → 50ohm does not help on reads that much
- For one slot population, even 150ohm seems O.K.

ODT value	2R 2R	2R 2R	2R 1R	2R 1R	1R 2R	1R 2R
150 ohm						
75 ohm						
50 ohm						
ODT value	**1R 1R**	**1R 1R**	**2R X**	**X 2R**	**1R X**	**X 1R**
150 ohm						
75 ohm						
50 ohm						

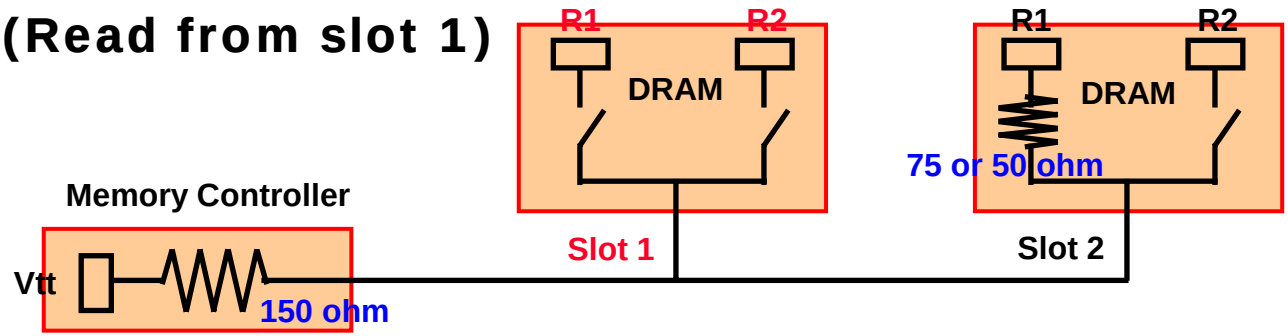
Recommended ODT Control - Reads

❑ Termination Matrix for Reads to DRAM

Configuration	Read from	Target DQ ODT Resistance RTT				
		Controller	Module in slot 1		Module in slot 2	
			Rank 1	Rank 2	Rank 1	Rank 2
2R 2R	slot 1	150 ohm	Infinite	Infinite	75 or 50 ohm	Infinite
	slot 2	150 ohm	75 or 50 ohm	Infinite	Infinite	Infinite
2R 1R	slot 1	150 ohm	Infinite	Infinite	75 or 50 ohm	Unpopulated
	slot 2	150 ohm	75 or 50 ohm	Infinite	Infinite	Unpopulated
1R 2R	slot 1	150 ohm	Infinite	Unpopulated	75 or 50 ohm	Infinite
	slot 2	150 ohm	75 or 50 ohm	Unpopulated	Infinite	Infinite
1R 1R	slot 1	150 ohm	Infinite	Unpopulated	75 or 50 ohm	Unpopulated
	slot 2	150 ohm	75 or 50 ohm	Unpopulated	Infinite	Unpopulated
2R Empty	slot 1	75 ohm	Infinite	Infinite	Unpopulated	Unpopulated
Empty 2R	slot 2	75 ohm	Unpopulated	Unpopulated	Infinite	Infinite
1R Empty	slot 1	75 ohm	Infinite	Unpopulated	Unpopulated	Unpopulated
Empty 1R	slot 2	75 ohm	Unpopulated	Unpopulated	Infinite	Unpopulated

❑ ODT on a controller always turned-on

❑ Example : 2R 2R (Read from slot 1)



Summary of ODT Control

- **ODT value should be decided depending on channel environment and set during initialization sequence**
  - ✓ For one slot/channel implementation, 150ohm seems O.K.
  - ✓ For two slots/channel implementation, ODT value need to be determined properly
  - ✓ For DDR2-400/533, 75ohm seems O.K.
  - ✓ For DDR2-667/800, 50ohm is better than 75ohm
- **ODT trun-on/off is controlled by ODT pin**
- **There're more possible termination methods, but not covered in this material**
  - ✓ For example, 37.5ohm termination is possible with both ODTs turned-on on a dual rank DIMM, which may result "better signal integrity, but relatively small voltage swing and more power consumption."