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Your license to speed™

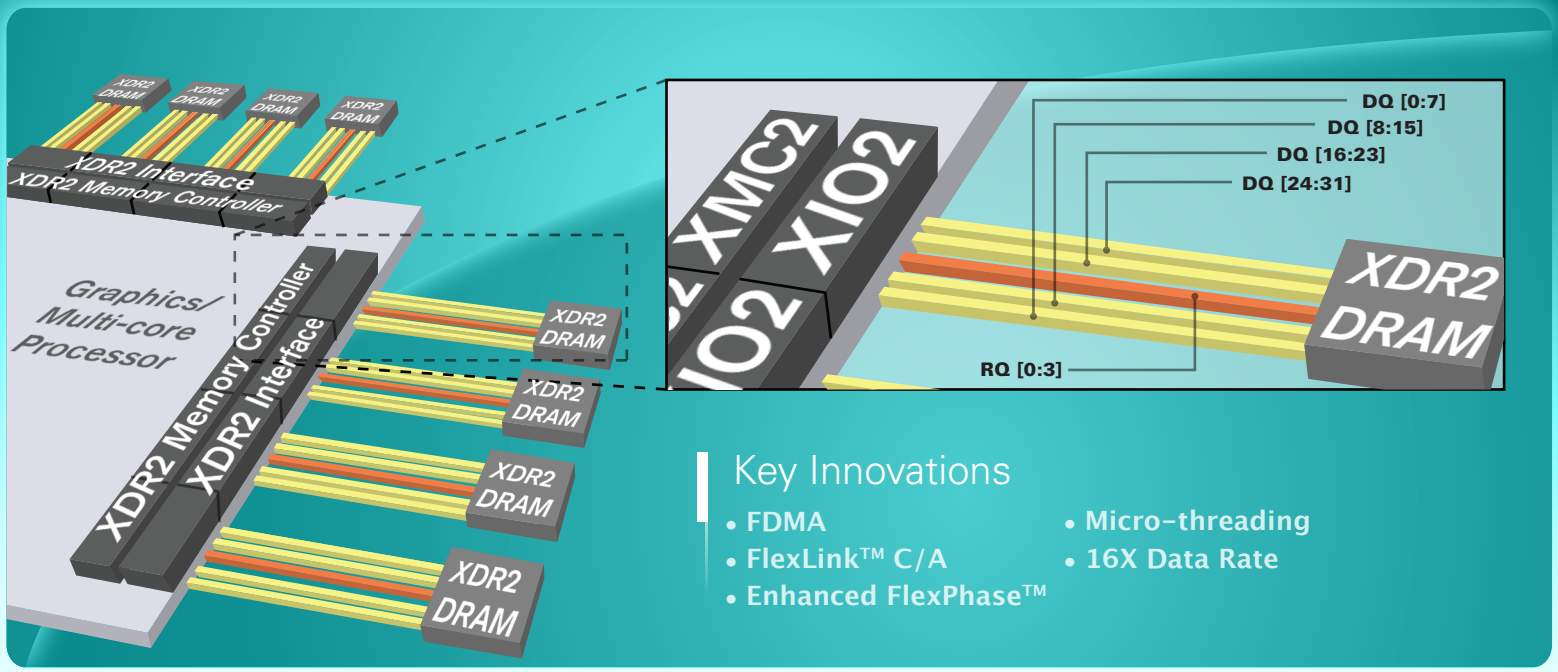
XDR™2 MEMORY ARCHITECTURE

Applications

- Graphics
- Gaming
- Multi-core Computing

Benefits

- Highest memory performance with reduced power and improved signal integrity
- Scalable system architecture with increased memory transfer efficiency
- Improved system yield and reduced system level costs



Key Innovations

- FDMA
- FlexLink™ C/A
- Enhanced FlexPhase™
- Micro-threading
- 16X Data Rate

XDR™2 is the World's Fastest DRAM Technology

Today's powerful graphics and multi-core processors require significantly higher memory performance when compared to traditional single-core processors. Without adequate data bandwidth, memory becomes the limiting factor in delivering the performance desired in next-generation gaming, graphics and computing systems. As an example, the current generation of gaming systems require up to 50GB/s of memory bandwidth. Current graphics processors need as much as 128GB/s. Over the course of the next five years, gaming, graphics, and multi-core computing applications are forecasted to push memory bandwidth requirements to 500GB/s and beyond.

To address these enormous bandwidth needs, Rambus has introduced the XDR2 memory architecture, the world's fastest DRAM technology, delivering data rates of up to 12.8Gbps. Featuring innovations such as Full Differential Memory Architecture (FDMA), FlexLink™ C/A, Micro-threading, and 16X data rate technology, XDR2 is capable of an astounding 51.2GB/s of bandwidth from a single XDR2 DRAM device. This dramatically exceeds the bandwidth capabilities of GDDR5 or DDR3 devices. Further, these Rambus innovations enable smaller memory controller interfaces and lower pin-counts while minimizing the total memory system bill-of-materials.

Innovative Features

The XDR2 memory architecture features innovations developed in Rambus' Terabyte Bandwidth Initiative (TBI). Fully Differential Memory Architecture (FDMA), one of many TBI innovations implemented in the XDR2 architecture, enables ultra-high speed data rates while reducing power and improving signal integrity. Another innovation, FlexLink C/A, enables scalable memory capacity and reduces system level costs. The XDR2 architecture features both the world's fastest data rate in a DRAM, and high transfer efficiency. Using Rambus Micro-threading technology, XDR2 memory delivers the performance of a 16-bank DRAM with a standard 8-bank CMOS DRAM core.

Total System Solution

The XDR2 controller interface cell is backward compatible with XDR DRAM devices providing system and chip designers the flexibility to develop controllers spanning multiple products and levels of performance.

As with XDR memory, the XDR2 architecture provides a total system solution addressing many of the complex issues faced by engineers designing cost effective, high-performance memory subsystems. XDR2 memory architecture is a best-in-class solution for applications that demand the highest levels of performance.

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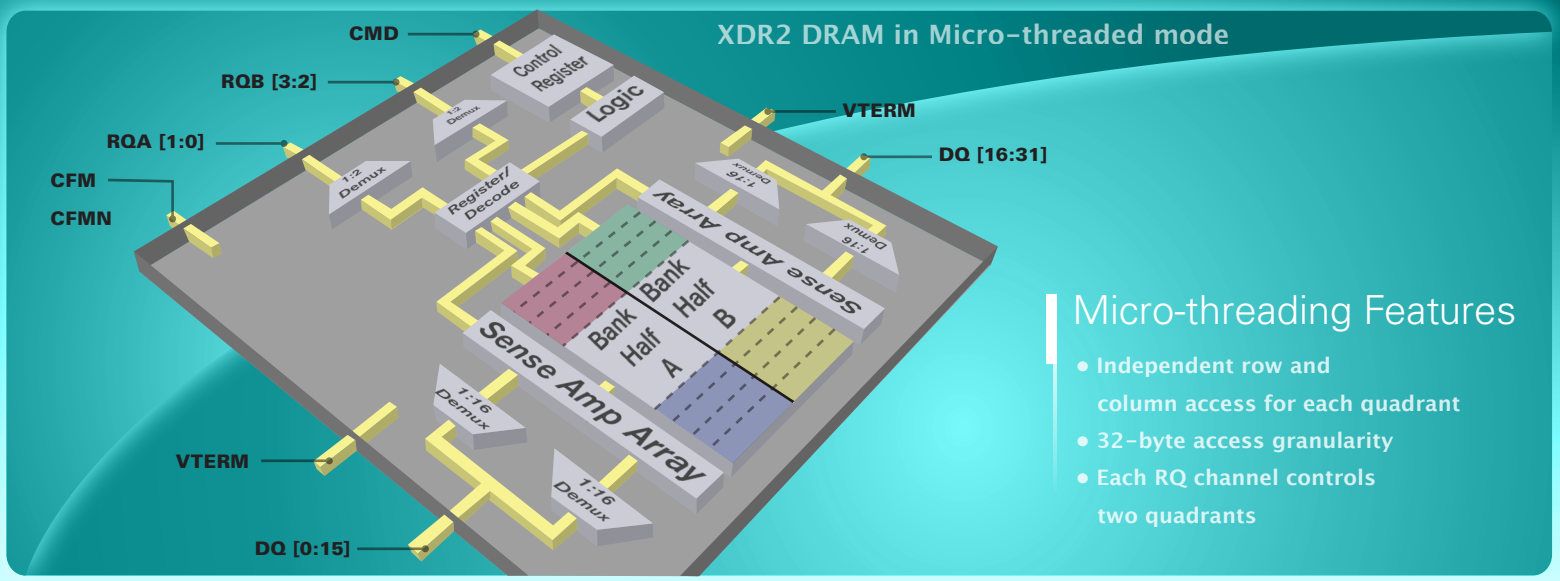
Features

Highest pin bandwidth
- 6.4 – 12.8Gbps data rate
- Enhanced FlexPhase™
- Asymmetric equalization

Highest sustained device bandwidth
- 25.6 – 51.2GB/s sustained data rate
- Micro-threaded 8-bank DRAM core
- 32-byte access granularity

Low power
- FlexLink C/A
- 1.5V Vdd
- Dynamic data width support



Micro-threading Features
- Independent row and column access for each quadrant
- 32-byte access granularity
- Each RQ channel controls two quadrants

Fully Differential Memory Architecture

Differential signaling improves data rates and power efficiency when compared with single-ended signaling techniques. Rambus pioneered high-speed differential signaling the first implementing this technology in the XDR memory architecture. The XDR2 architecture takes this approach to its ultimate extent with the implementation of the first Fully Differential Memory Architecture (FDMA). The XDR2 architecture employs differential signaling on all key signal connections between the memory controller and the DRAM: data, clock and command/address. Differential signaling inherently reduces noise, such as simultaneous switching output (SSO), crosstalk, and electromagnetic interference (EMI).

FlexLink Command and Address

The XDR2 architecture features FlexLink C/A, the industry's first full-speed, scalable point-to-point command/address channel. FlexLink C/A provides the command and address information to a DRAM using a single, high-speed differential communications channel. Operating at up to 12.8Gbps in the XDR2 architecture, FlexLink C/A reduces the required number of signal pins on both the DRAM and the memory controller. In contrast with a 1Gbit GDDR5 device which requires 15 wires for its C/A link, FlexLink C/A implements a full 12.8Gbps C/A link with one differential pair. This serial, scalable link also provides fine access and scalable capacity through a single command/address link per XDR2 DRAM. FlexLink C/A's serial connectivity reduces die and PCB area, decreases power and pin count, and lowers overall system costs.

Micro-threading Technology

Most DRAM cores divide memory storage into discrete banks that can be accessed concurrently. Banks are typically split across both rows of the DRAM die. Since DRAM pins are also split across the two halves, each half-bank delivers its data to its corresponding pins.

Each time a row within a bank is accessed, the core dedicates resources on both sides of the DRAM. Micro-threading splits each bank in half and makes each independently addressable. In this way, a traditional 8-bank CMOS core operates as a 16-bank core with micro-threading. Interleaving transactions between the banks can yield 32-byte access granularity with a sustained bandwidth of up to 51.2GB/s. Reduced row and column access granularity results in a significant performance benefit for applications dealing with small data objects as commonly found in graphics and gaming applications. Furthermore, independent addressability of each DRAM quadrant improves transfer efficiency in multi-core computing applications.

16X Data Rate Technology

Rambus' innovative 16X data rate technology transmits 16 bits of data per clock cycle on each I/O. Conventional double data rate memory systems transfer only two bits of data per I/O during every clock cycle. With 16X data rate technology, incredibly high signaling speeds can be achieved while maintaining relatively low system clock speeds. For example, the XDR 2 architecture can operate at 12.8Gbps with only an 800MHz system clock. Lower system clock speeds simplify design considerations and minimize manufacturing costs.