Chapter 24

SD16_A

The SD16_A module is a single-converter 16-bit, sigma-delta analog-to-digital conversion module with high impedance input buffer. This chapter describes the SD16_A. The SD16_A module is implemented in the MSP430x20x3 devices.

Topic **Page**

24.1 SD16_A Introduction

The SD16_A module consists of one sigma-delta analog-to-digital converter with a high-impedance input buffer and an internal voltage reference. It has up to eight fully differential multiplexed analog input pairs including a built-in temperature sensor and a divided supply voltage. The converter is based on a second-order oversampling sigma-delta modulator and digital decimation filter. The decimation filter is a comb type filter with selectable oversampling ratios of up to 1024. Additional filtering can be done in software.

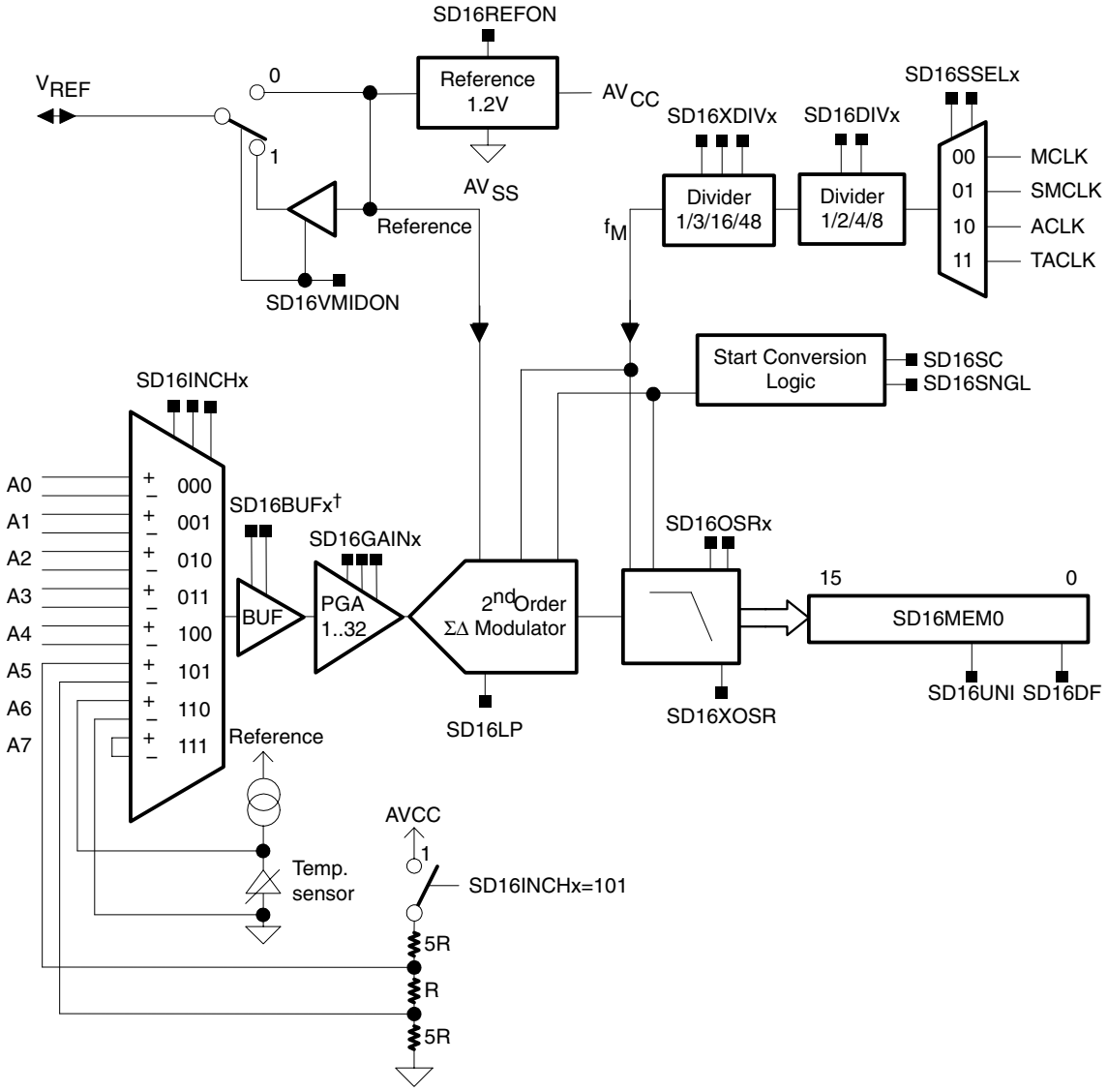
The high impedance input buffer is not implemented in MSP430x20x3 devices.

Features of the SD16_A include:

- 16-bit sigma-delta architecture
- Up to eight multiplexed differential analog inputs per channel
  (The number of inputs is device dependent, see the device-specific data sheet.)
- Software selectable on-chip reference voltage generation (1.2V)
- Software selectable internal or external reference
- Built-in temperature sensor
- Up to 1.1 MHz modulator input frequency
- High impedance input buffer
  (not implemented on all devices, see the device-specific data sheet)
- Selectable low-power conversion mode

The block diagram of the SD16_A module is shown in Figure 24–1.

Figure 24−1. SD16_A Block Diagram



† Not Implemented in MSP430x20x3 devices

24.2 SD16_A Operation

The SD16_A module is configured with user software. The setup and operation of the SD16_A is discussed in the following sections.

24.2.1 ADC Core

The analog-to-digital conversion is performed by a 1-bit second-order sigma-delta modulator. A single-bit comparator within the modulator quantizes the input signal with the modulator frequency f_M. The resulting 1-bit data stream is averaged by the digital filter for the conversion result.

24.2.2 Analog Input Range and PGA

The full-scale input voltage range for each analog input pair is dependent on the gain setting of the programmable gain amplifier of each channel. The maximum full-scale range is $\pm V_{FSR}$ where V_{FSR} is defined by:

$$V_{FSR} = \frac{V_{REF}/2}{GAIN_{PGA}}$$

For a 1.2V reference, the maximum full-scale input range for a gain of 1 is:

$$\pm\ V_{FSR} = \frac{1.2V/2}{1} = \pm\ 0.6V$$

See the device-specific data sheet for full-scale input specifications.

24.2.3 Voltage Reference Generator

The SD16_A module has a built-in 1.2V reference. It is enabled by the SD16REFON bit. When using the internal reference an external 100-nF capacitor connected from V_{REF} to AV_{SS} is recommended to reduce noise. The internal reference voltage can be used off-chip when SD16VMIDON = 1. The buffered output can provide up to 1mA of drive. When using the internal reference off-chip, a 470-nF capacitor connected from V_{REF} to AV_{SS} is required. See the device-specific data sheet for parameters.

An external voltage reference can be applied to the V_{REF} input when SD16REFON and SD16VMIDON are both reset.

24.2.4 Auto Power-Down

The SD16_A is designed for low power applications. When the SD16_A is not actively converting, it is automatically disabled and automatically re-enabled when a conversion is started. The reference is not automatically disabled, but can be disabled by setting SD16REFON = 0. When the SD16_A or reference are disabled, they consume no current.

24.2.5 Analog Input Pair Selection

The SD16_A can convert up to 8 differential input pairs multiplexed into the PGA. Up to five analog input pairs (A0-A4) are available externally on the device. A resistive divider to measure the supply voltage is available using the A5 multiplexer input. An internal temperature sensor is available using the A6 multiplexer input. Input A7 is a shorted connection between the + and – input pair and can be used to calibrate the offset of the SD16_A input stage.

Analog Input Setup

The analog input is configured using the SD16INCTL0 and the SD16AE registers. The SD16INCHx bits select one of eight differential input pairs of the analog multiplexer. The gain for the PGA is selected by the SD16GAINx bits. A total of six gain settings are available. The SD16AEx bits enable or disable the analog input pin. Setting any SD16AEx bit disables the multiplexed digital circuitry for the associated pin. See the device-specific data sheet for pin diagrams.

During conversion any modification to the SD16INCHx and SD16GAINx bits will become effective with the next decimation step of the digital filter. After these bits are modified, the next three conversions may be invalid due to the settling time of the digital filter. This can be handled automatically with the SD16INTDLYx bits. When SD16INTDLY = 00h, conversion interrupt requests will not begin until the 4^{th} conversion after a start condition.

On devices implementing the high impedance input buffer it can be enabled using the SD16BUFx bits. The speed settings are selected based on the SD16_A modulator frequency as shown in Table 24–1.

Table 24–1. High Input Impedance Buffer

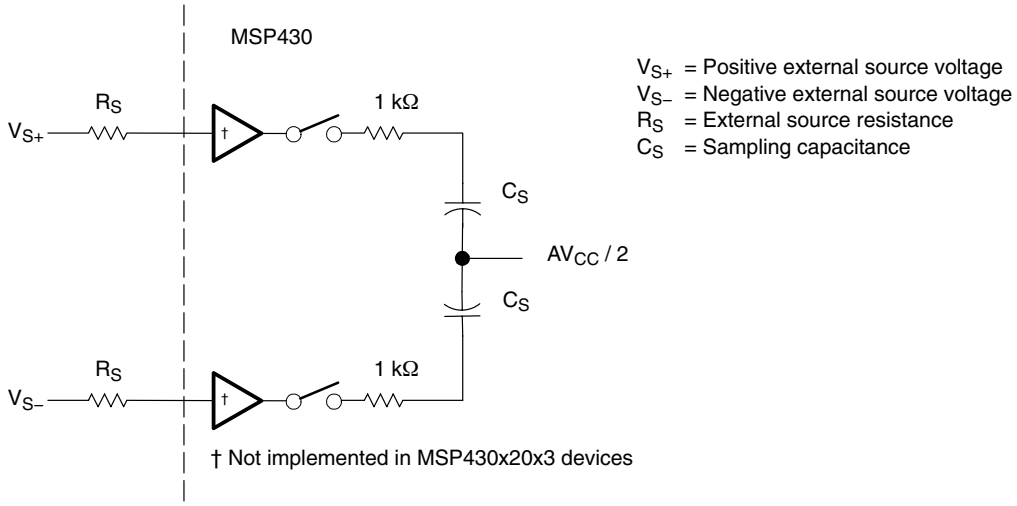
SD16BUFx	Buffer	SD16 Modulator Frequency f_M
00	Buffer disabled	
01	Low speed/current	f_M < 200kHz
10	Medium speed/current	200kHz < f_M < 700kHz
11	High speed/current	700kHz < f_M < 1.1MHz

An external RC anti-aliasing filter is recommended for the SD16_A to prevent aliasing of the input signal. The cutoff frequency should be < 10 kHz for a 1-Mhz modulator clock and OSR = 256. The cutoff frequency may set to a lower frequency for applications that have lower bandwidth requirements.

24.2.6 Analog Input Characteristics

The SD16_A uses a switched-capacitor input stage that appears as an impedance to external circuitry as shown in Figure 24–2.

Figure 24–2. Analog Input Equivalent Circuit



When the buffers are used, R_S does not affect the sampling frequency f_S. However, when the buffers are not used or are not present on the device, the maximum sampling frequency f_S may be calculated from the minimum settling time $t_{Settling}$ of the sampling circuit given by:

$$t_{Settling} \geq (R_S + 1k\Omega) \times C_S \times \ln\left(\frac{GAIN \times 2^{17} \times V_{Ax}}{V_{REF}}\right)$$

where

$$f_S = \frac{1}{2 \times t_{Settling}} \text{ and } V_{Ax} = \max\left(\left|\frac{AV_{CC}}{2} - V_{S+}\right|, \left|\frac{AV_{CC}}{2} - V_{S-}\right|\right),$$

with V_{S+} and V_{S-} referenced to AV_{SS}.

C_S varies with the gain setting as shown in Table 24–2.

Table 24–2. Sampling Capacitance

PGA Gain	Sampling Capacitance C_S
1	1.25 pF
2, 4	2.5 pF
8	5 pF
16, 32	10 pF

24.2.7 Digital Filter

The digital filter processes the 1-bit data stream from the modulator using a SINC^3 comb filter. The transfer function is described in the z-Domain by:

$$H(z) = \left(\frac{1}{OSR} \times \frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3$$

and in the frequency domain by:

$$H(f) = \left[\frac{sinc\left(OSR\pi \frac{f}{f_M}\right)}{sinc\left(\pi \frac{f}{f_M}\right)}\right]^3 = \left[\frac{1}{OSR} \times \frac{\sin\left(OSR \times \pi \times \frac{f}{f_M}\right)}{\sin\left(\pi \times \frac{f}{f_M}\right)}\right]^3$$

where the oversampling rate, OSR, is the ratio of the modulator frequency f_M to the sample frequency f_S. Figure 24–3 shows the filter's frequency response for an OSR of 32. The first filter notch is at $f_S = f_M/OSR$. The notch's frequency can be adjusted by changing the modulator's frequency, f_M, using SD16SSELx and SD16DIVx and the oversampling rate using the SD16OSRx and SD16XOSR bits.

The digital filter for each enabled ADC channel completes the decimation of the digital bit-stream and outputs new conversion results to the SD16MEM0 register at the sample frequency f_S.

Figure 24–3. Comb Filter's Frequency Response with OSR = 32

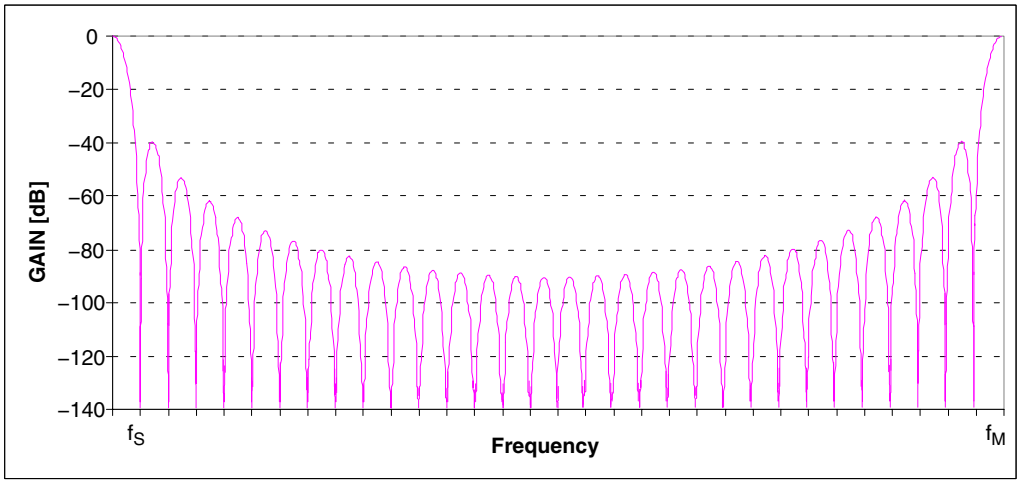
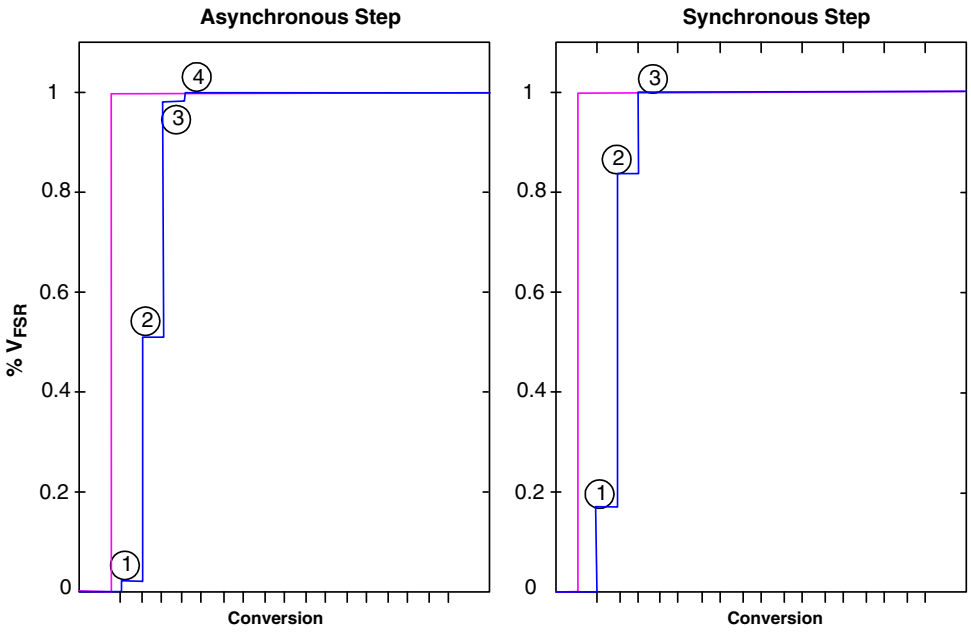


Figure 24–4 shows the digital filter step response and conversion points. For step changes at the input after start of conversion a settling time must be allowed before a valid conversion result is available. The SD16INTDLYx bits can provide sufficient filter settling time for a full-scale change at the ADC input. If the step occurs synchronously to the decimation of the digital filter the valid data will be available on the third conversion. An asynchronous step will require one additional conversion before valid data is available.

Figure 24–4. Digital Filter Step Response and Conversion Points



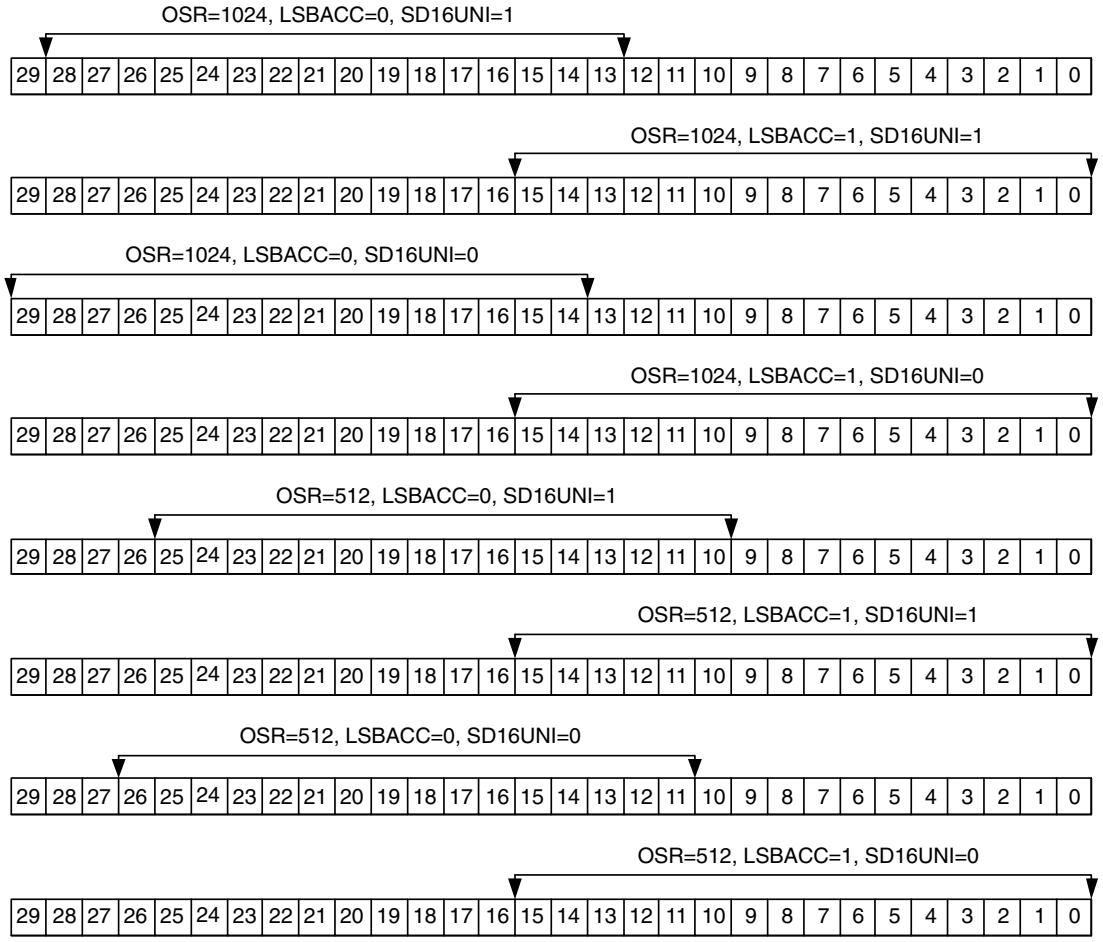
Digital Filter Output

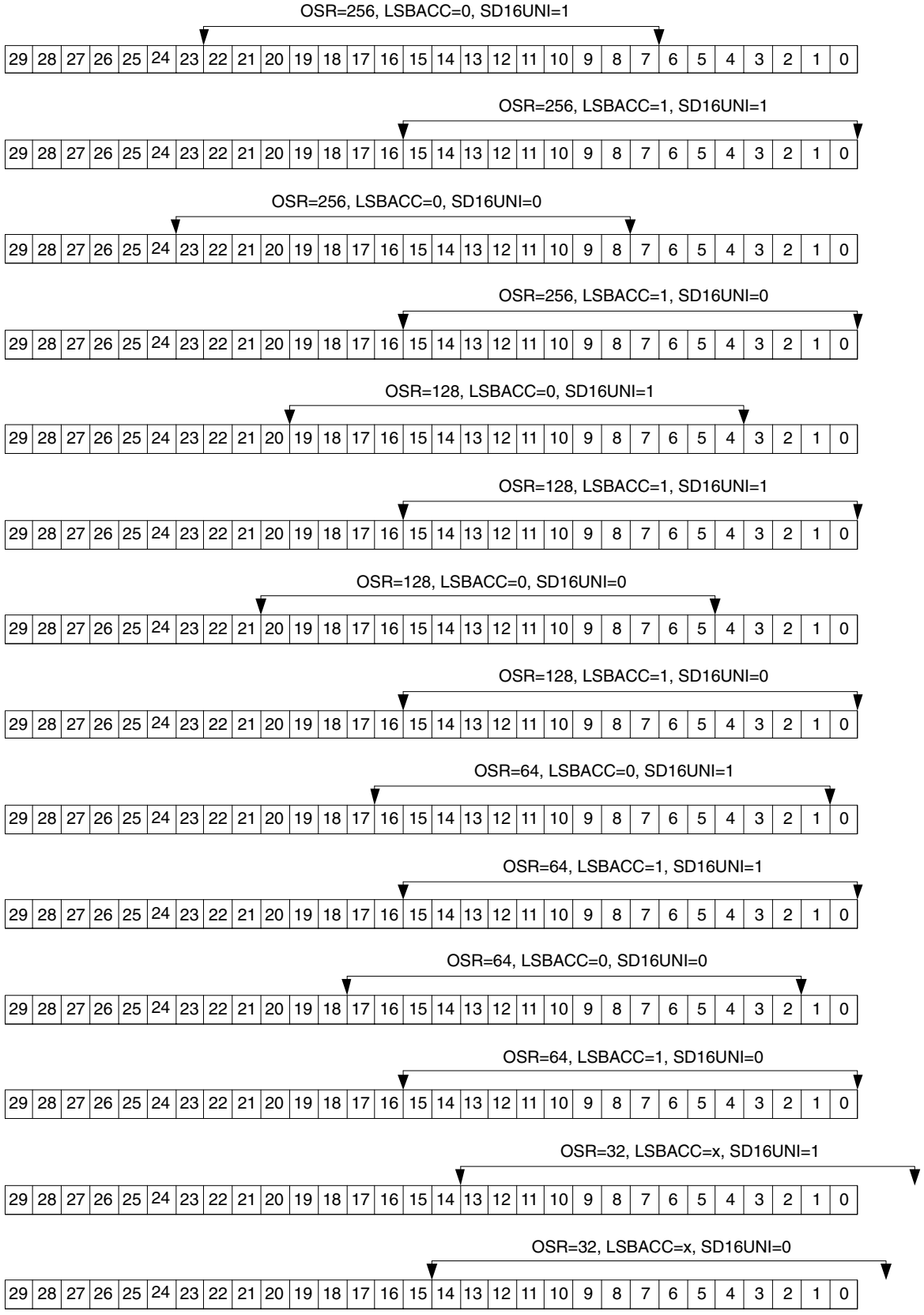
The number of bits output by the digital filter is dependent on the oversampling ratio and ranges from 15 to 30 bits. Figure 24–5 shows the digital filter output and their relation to SD16MEM0 for each OSR, LSBACC, and SD16UNI setting. For example, for OSR = 1024, LSBACC = 0, and SD16UNI = 1, the SD16MEM0 register contains bits 28 – 13 of the digital filter output. When OSR = 32, the one (SD16UNI = 0) or two (SD16UNI=1) LSBs are always zero.

The SD16LSBACC and SD16LSBTOG bits give access to the least significant bits of the digital filter output. When SD16LSBACC = 1 the 16 least significant bits of the digital filter's output are read from SD16MEM0 using word instructions. The SD16MEM0 register can also be accessed with byte instructions returning only the 8 least significant bits of the digital filter output.

When SD16LSBTOG = 1 the SD16LSBACC bit is automatically toggled each time SD16MEM0 is read. This allows the complete digital filter output result to be read with two reads of SD16MEM0. Setting or clearing SD16LSBTOG does not change SD16LSBACC until the next SD16MEM0 access.

Figure 24–5. Used Bits of Digital Filter Output




OSR=256, LSBACC=0, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=256, LSBACC=1, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=256, LSBACC=0, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=256, LSBACC=1, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=128, LSBACC=0, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=128, LSBACC=1, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=128, LSBACC=0, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=128, LSBACC=1, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=64, LSBACC=0, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=64, LSBACC=1, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=64, LSBACC=0, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=64, LSBACC=1, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=32, LSBACC=x, SD16UNI=1
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OSR=32, LSBACC=x, SD16UNI=0
29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

24.2.8 Conversion Memory Register: SD16MEM0

The SD16MEM0 register is associated with the SD16_A channel. Conversion results are moved to the SD16MEM0 register with each decimation step of the digital filter. The SD16IFG bit is set when new data is written to SD16MEM0. SD16IFG is automatically cleared when SD16MEM0 is read by the CPU or may be cleared with software.

Output Data Format

The output data format is configurable in two's complement, offset binary or unipolar mode as shown in Table 24–3.The data format is selected by the SD16DF and SD16UNI bits.

Table 24–3.Data Format

SD16UNI	SD16DF	Format	Analog Input	SD16MEM0†	Digital Filter Output (OSR = 256)
0	0	Bipolar Offset Binary	+FSR	FFFF	FFFFFF
			ZERO	8000	800000
			–FSR	0000	000000
0	1	Bipolar Twos compliment	+FSR	7FFF	7FFFFF
			ZERO	0000	000000
			–FSR	8000	800000
1	0	Unipolar	+FSR	FFFF	FFFFFF
			ZERO	0000	800000
			–FSR	0000	000000

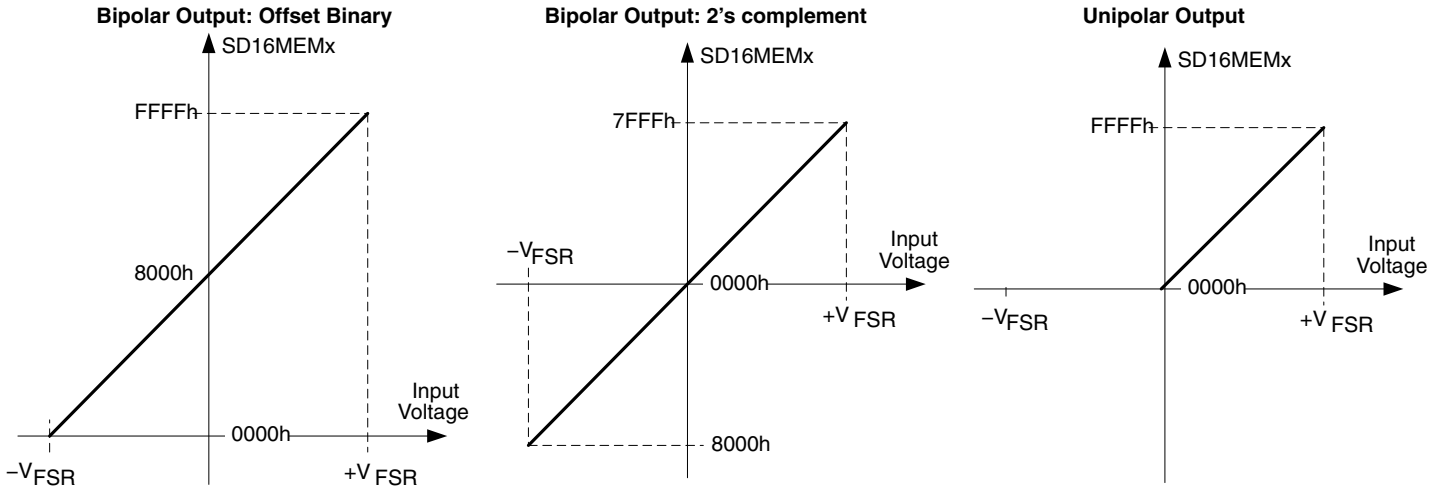
† Independent of SD16OSRx and SD16XOSR settings; SD16LSBACC = 0.

Note: Offset Measurements and Data Format

Any offset measurement done either externally or using the internal differential pair A7 would be appropriate only when the channel is operating under bipolar mode with SD16UNI = 0.

Figure 24–6 shows the relationship between the full-scale input voltage range from $-V_{FSR}$ to $+V_{FSR}$ and the conversion result. The data formats are illustrated.

Figure 24–6. Input Voltage vs. Digital Output



24.2.9 Conversion Modes

The SD16_A module can be configured for two modes of operation, listed in Table 24–4. The SD16SNGL bit selects the conversion mode.

Table 24–4. Conversion Mode Summary

SD16SNGL	Mode	Operation
1	Single conversion	The channel is converted once.
0	Continuous conversion	The channel is converted continuously.

Single Conversion

Setting the SD16SC bit of the channel initiates one conversion on that channel when SD16SNGL = 1. The SD16SC bit will automatically be cleared after conversion completion.

Clearing SD16SC before the conversion is completed immediately stops conversion of the channel, the channel is powered down and the corresponding digital filter is turned off. The value in SD16MEM0 can change when SD16SC is cleared. It is recommended that the conversion data in SD16MEM0 be read prior to clearing SD16SC to avoid reading an invalid result.

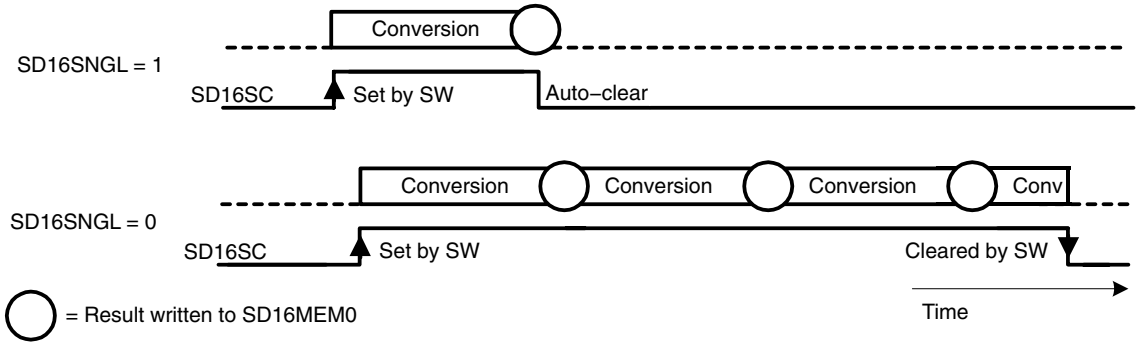
Continuous Conversion

When SD16SNGL = 0 continuous conversion mode is selected. Conversion of the channel will begin when SD16SC is set and continue until the SD16SC bit is cleared by software.

Clearing SD16SC immediately stops conversion of the selected channel, the channel is powered down and the corresponding digital filter is turned off. The value in SD16MEM0 can change when SD16SC is cleared. It is recommended that the conversion data in SD16MEM0 be read prior to clearing SD16SC to avoid reading an invalid result.

Figure 24–7 shows conversion operation.

Figure 24–7. Single Channel Operation

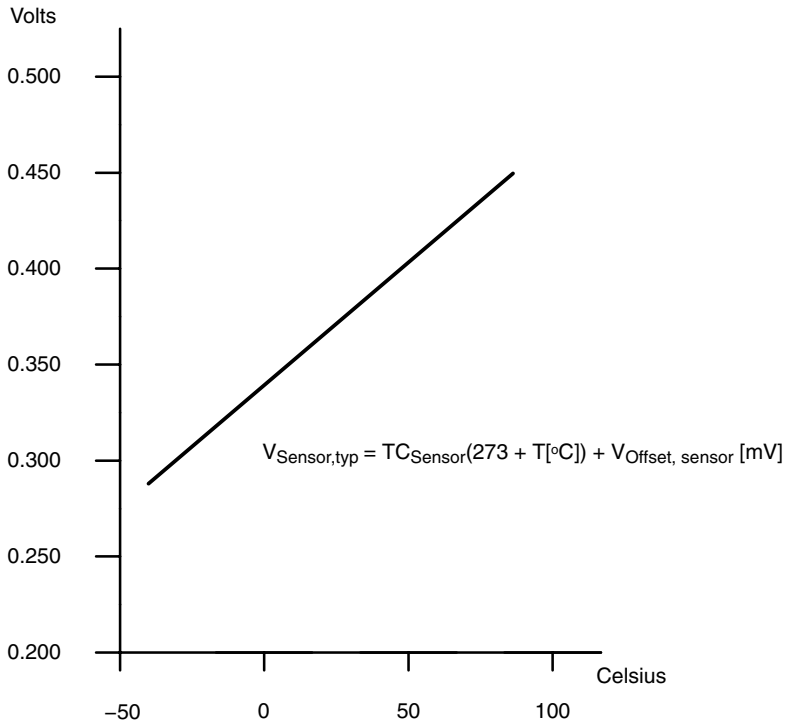


24.2.10 Using the Integrated Temperature Sensor

To use the on-chip temperature sensor, the user selects the analog input pair SD16INCHx = 110 and sets SD16REFON = 1. Any other configuration is done as if an external analog input pair was selected, including SD16INTDLYx and SD16GAINx settings. Because the internal reference must be on to use the temperature sensor, it is not possible to use an external reference for the conversion of the temperature sensor voltage. Also, the internal reference will be in contention with any used external reference. In this case, the SD16VMIDON bit may be set to minimize the affects of the contention on the conversion.

The typical temperature sensor transfer function is shown in Figure 24–8. When switching inputs of an SD16_A channel to the temperature sensor, adequate delay must be provided using SD16INTDLYx to allow the digital filter to settle and assure that conversion results are valid. The temperature sensor offset error can be large, and may need to be calibrated for most applications. See device-specific data sheet for temperature sensor parameters.

Figure 24–8. Typical Temperature Sensor Transfer Function



24.2.11 Interrupt Handling

The SD16_A has 2 interrupt sources for its ADC channel:

- SD16IFG
- SD16OVIFG

The SD16IFG bit is set when the SD16MEM0 memory register is written with a conversion result. An interrupt request is generated if the corresponding SD16IE bit and the GIE bit are set. The SD16_A overflow condition occurs when a conversion result is written to SD16MEM0 location before the previous conversion result was read.

SD16IV, Interrupt Vector Generator

All SD16_A interrupt sources are prioritized and combined to source a single interrupt vector. SD16IV is used to determine which enabled SD16_A interrupt source requested an interrupt. The highest priority SD16_A interrupt request that is enabled generates a number in the SD16IV register (see register description). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled SD16_A interrupts do not affect the SD16IV value.

Any access, read or write, of the SD16IV register has no effect on the SD16OVIFG or SD16IFG flags. The SD16IFG flags are reset by reading the SD16MEM0 register or by clearing the flags in software. SD16OVIFG bits can only be reset with software.

If another interrupt is pending after servicing of an interrupt, another interrupt is generated. For example, if the SD16OVIFG and one or more SD16IFG interrupts are pending when the interrupt service routine accesses the SD16IV register, the SD16OVIFG interrupt condition is serviced first and the corresponding flag(s) must be cleared in software. After the RETI instruction of the interrupt service routine is executed, the highest priority SD16IFG pending generates another interrupt request.

Interrupt Delay Operation

The SD16INTDLYx bits control the timing for the first interrupt service request for the corresponding channel. This feature delays the interrupt request for a completed conversion by up to four conversion cycles allowing the digital filter to settle prior to generating an interrupt request. The delay is applied each time the SD16SC bit is set or when the SD16GAINx or SD16INCHx bits for the channel are modified. SD16INTDLYx disables overflow interrupt generation for the channel for the selected number of delay cycles. Interrupt requests for the delayed conversions are not generated during the delay.

24.3 SD16_A Registers

The SD16_A registers are listed in Table 24–5:

Table 24–5. SD16_A Registers

Register	Short Form	Register Type	Address	Initial State
SD16_A control	SD16CTL	Read/write	0100h	Reset with PUC
SD16_A interrupt vector	SD16IV	Read/write	0110h	Reset with PUC
SD16_A channel 0 control	SD16CCTL0	Read/write	0102h	Reset with PUC
SD16_A conversion memory	SD16MEM0	Read/write	0112h	Reset with PUC
SD16_A input control	SD16INCTL0	Read/write	0B0h	Reset with PUC
SD16_A analog enable	SD16AE	Read/write	0B7h	Reset with PUC

SD16CTL, SD16_A Control Register

15	14	13	12	11	10	9	8
Reserved				SD16XDIVx			SD16LP
r0	r0	r0	r0	rw–0	rw–0	rw–0	rw–0

7	6	5	4	3	2	1	0
SD16DIVx		SD16SSELx		SD16 VMIDON	SD16 REFON	SD16OVIE	Reserved
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	r0

Reserved Bits 15-12 Reserved

SD16XDIVx Bits 11-9 SD16_A clock divider
- 000 /1
- 001 /3
- 010 /16
- 011 /48
- 1xx Reserved

SD16LP Bit 8 Low power mode. This bit selects a reduced speed, reduced power mode
- 0 Low-power mode is disabled
- 1 Low-power mode is enabled. The maximum clock frequency for the SD16_A is reduced.

SD16DIVx Bits 7-6 SD16_A clock divider
- 00 /1
- 01 /2
- 10 /4
- 11 /8

SD16SSELx Bits 5-4 SD16_A clock source select
- 00 MCLK
- 01 SMCLK
- 10 ACLK
- 11 External TACLK

SD16 VMIDON Bit 3 V_{MID} buffer on
- 0 Off
- 1 On

SD16 REFON Bit 2 Reference generator on
- 0 Reference off
- 1 Reference on

SD16OVIE Bit 1 SD16_A overflow interrupt enable. The GIE bit must also be set to enable the interrupt.
- 0 Overflow interrupt disabled
- 1 Overflow interrupt enabled

Reserved Bit 0 Reserved

SD16CCTL0, SD16_A Control Register 0

15	14	13	12	11	10	9	8
Reserved	SD16BUFx†		SD16UNI	SD16XOSR	SD16SNGL	SD16OSRx	
r0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

7	6	5	4	3	2	1	0
SD16 LSBTOG	SD16 LSBACC	SD16 OVIFG	SD16DF	SD16IE	SD16IFG	SD16SC	Reserved
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	r–0

† Reserved in MSP430x20x3 devices

Reserved Bit 15 Reserved

SD16BUFx Bits 14–13 High-impedance input buffer mode
00 Buffer disabled
01 Slow speed/current
10 Medium speed/current
11 High speed/current

SD16UNI Bit 12 Unipolar mode select
0 Bipolar mode
1 Unipolar mode

SD16XOSR Bit 11 Extended oversampling ratio. This bit, along with the SD16OSRx bits, select the oversampling ratio. See SD16OSRx bit description for settings.

SD16SNGL Bit 10 Single conversion mode select
0 Continuous conversion mode
1 Single conversion mode

SD16OSRx Bits 9-8 Oversampling ratio
When SD16XOSR = 0
00 256
01 128
10 64
11 32
When SD16XOSR = 1
00 512
01 1024
10 Reserved
11 Reserved

SD16 LSBTOG Bit 7 LSB toggle. This bit, when set, causes SD16LSBACC to toggle each time the SD16MEM0 register is read.
0 SD16LSBACC does not toggle with each SD16MEM0 read
1 SD16LSBACC toggles with each SD16MEM0 read

SD16 LSBACC	Bit 6	LSB access. This bit allows access to the upper or lower 16-bits of the SD16_A conversion result. 0 SD16MEMx contains the most significant 16-bits of the conversion. 1 SD16MEMx contains the least significant 16-bits of the conversion.
SD16OVIFG	Bit 5	SD16_A overflow interrupt flag 0 No overflow interrupt pending 1 Overflow interrupt pending
SD16DF	Bit 4	SD16_A data format 0 Offset binary 1 2's complement
SD16IE	Bit 3	SD16_A interrupt enable 0 Disabled 1 Enabled
SD16IFG	Bit 2	SD16_A interrupt flag. SD16IFG is set when new conversion results are available. SD16IFG is automatically reset when the corresponding SD16MEMx register is read, or may be cleared with software. 0 No interrupt pending 1 Interrupt pending
SD16SC	Bit 1	SD16_A start conversion 0 No conversion start 1 Start conversion
Reserved	Bit 0	Reserved

SD16INCTL0, SD16_A Input Control Register

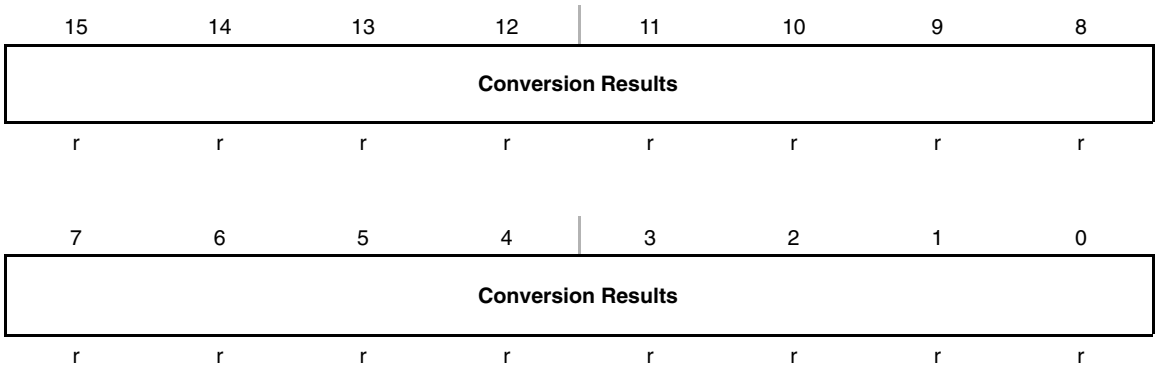
7	6	5	4	3	2	1	0
SD16INTDLYx		SD16GAINx			SD16INCHx		
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

SD16INTDLYx Bits 7-6 Interrupt delay generation after conversion start. These bits select the delay for the first interrupt after conversion start.
- 00 Fourth sample causes interrupt
- 01 Third sample causes interrupt
- 10 Second sample causes interrupt
- 11 First sample causes interrupt

SD16GAINx Bits 5-3 SD16_A preamplifier gain
- 000 x1
- 001 x2
- 010 x4
- 011 x8
- 100 x16
- 101 x32
- 110 Reserved
- 111 Reserved

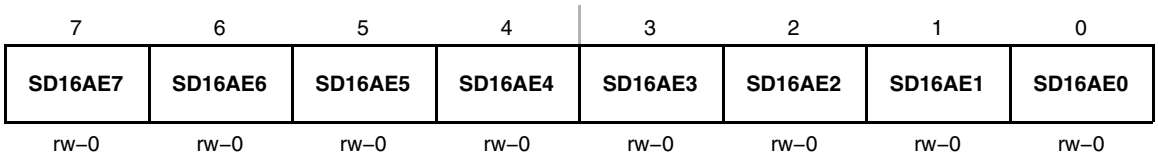
SD16INCHx Bits 2-0 SD16_A channel differential pair input
- 000 A0
- 001 A1
- 010 A2
- 011 A3
- 100 A4
- 101 A5– (AV_{CC} – AV_{SS}) / 11
- 110 A6 – Temperature Sensor
- 111 A7 – Short for PGA offset measurement

SD16MEM0, SD16_A Conversion Memory Register



Conversion Result Bits 15-0 Conversion Results. The SD16MEMx register holds the upper or lower 16-bits of the digital filter output, depending on the SD16LSBACC bit.

SD16AE, SD16_A Analog Input Enable Register



SD16AEx Bits 7-0 SD16_A analog enable
- 0 External input disabled. Negative inputs are internally connected to VSS.
- 1 External input enabled.

SD16IV, SD16_A Interrupt Vector Register

15	14	13	12	11	10	9	8
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
0	**0**	**0**	**SD16IVx**				**0**
r0	r0	r0	r–0	r–0	r–0	r–0	r0

SD16IVx Bits 15-0 SD16_A interrupt vector value

SD16IV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
000h	No interrupt pending	–	
002h	SD16MEMx overflow	SD16CCTLx SD16OVIFG	Highest
004h	SD16_A Interrupt	SD16CCTL0 SD16IFG	
006h	Reserved	–	
008h	Reserved	–	
00Ah	Reserved	–	
00Ch	Reserved	–	
00Eh	Reserved	–	
010h	Reserved	–	Lowest