16/32/64bit EISC Microprocessor

Advanced Digital Chips

An Embedded Microprocessor Company

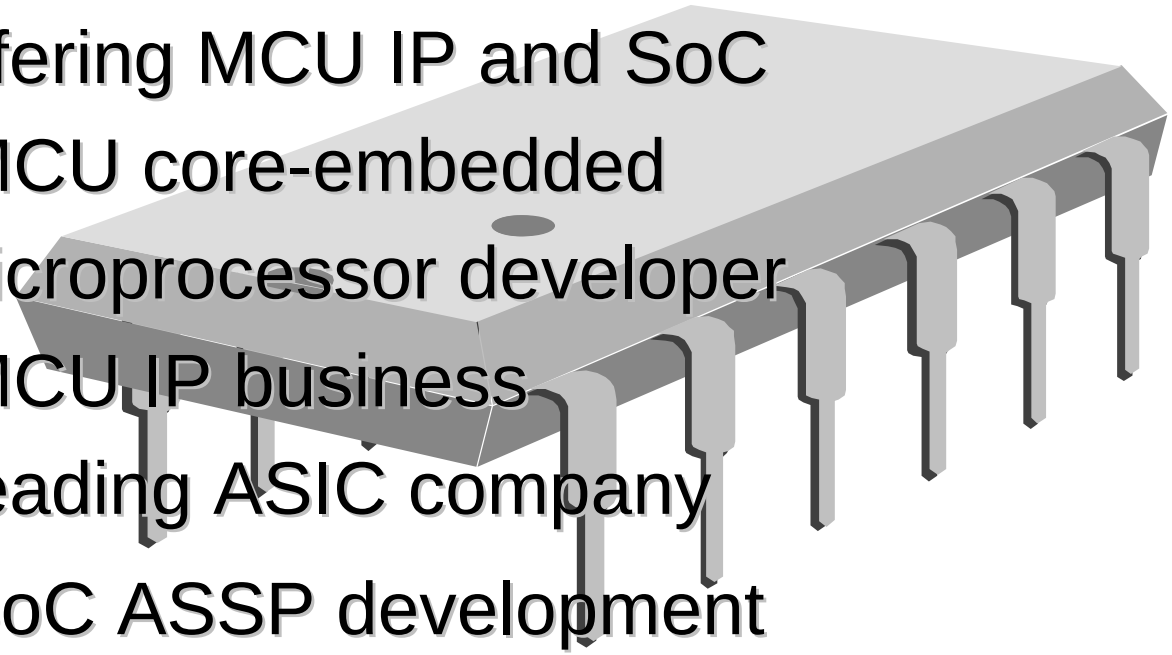
Mar. 2007

adc

adc
advanced digital chips inc.

adchips is .....

- a fabless semiconductor company offering MCU IP and SoC
- a MCU core-embedded microprocessor developer
- a MCU IP business
- a leading ASIC company
- a SoC ASSP development



Advanced Digital Chips (ADC), a Korean KOSDAQ company began developing a next generation CPU architecture technology in 1998.

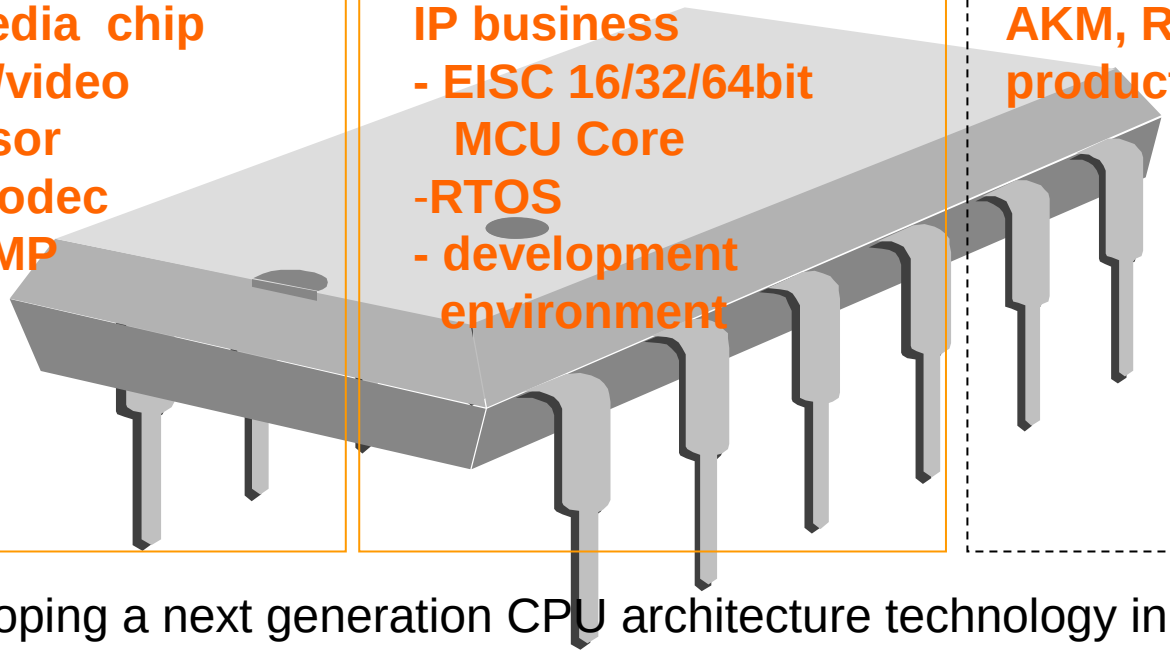
- This state of the art CPU, called EISC, is designed as a embedded MCU solution.

Company Overview

Business Units	:	**Semiconductor Design Company**
		- Multimedia/Consumer/Game System on Chip (SoC) ASSP Development
		- Intellectual Property (IP) Licensing
Location	:	**Seoul, Korea**
Overseas Presence	:	**Silicon Valley Subsidiary (March 2002)**
		Pennsylvania Subsidiary (September 2003)
		China Subsidiary (April 2006)
Founding Date	:	**April 16, 1996**
KOSDAQ Shares	:	**5,200,000 Shares @ 500 won par value**
Employees	:	**75 (30 Involved in R & D Related Activities)**

Business area

SoC ASSP business	MCU IP Business	Trading
1.Multimedia chip - graphic/video processor 2.H.264 codec - DMB/ PMP 3.Etc.	IP business - EISC 16/32/64bit MCU Core -RTOS - development environment	AKM, RICOH's products Trading

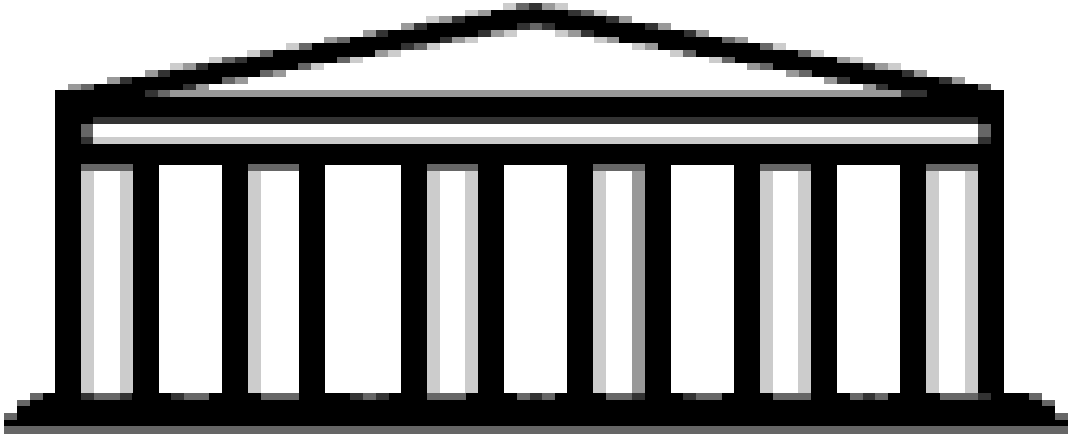


1. Developing a next generation CPU architecture technology in 1998 to offer a smaller, faster and cheaper solution.
2. ADC introduces the EISC technology to the industry in two ways, firstly through the sale of multimedia SoC incorporating the EISC MCU, and secondly by licensing its EISC MCU as IP .

Invention of new ISA

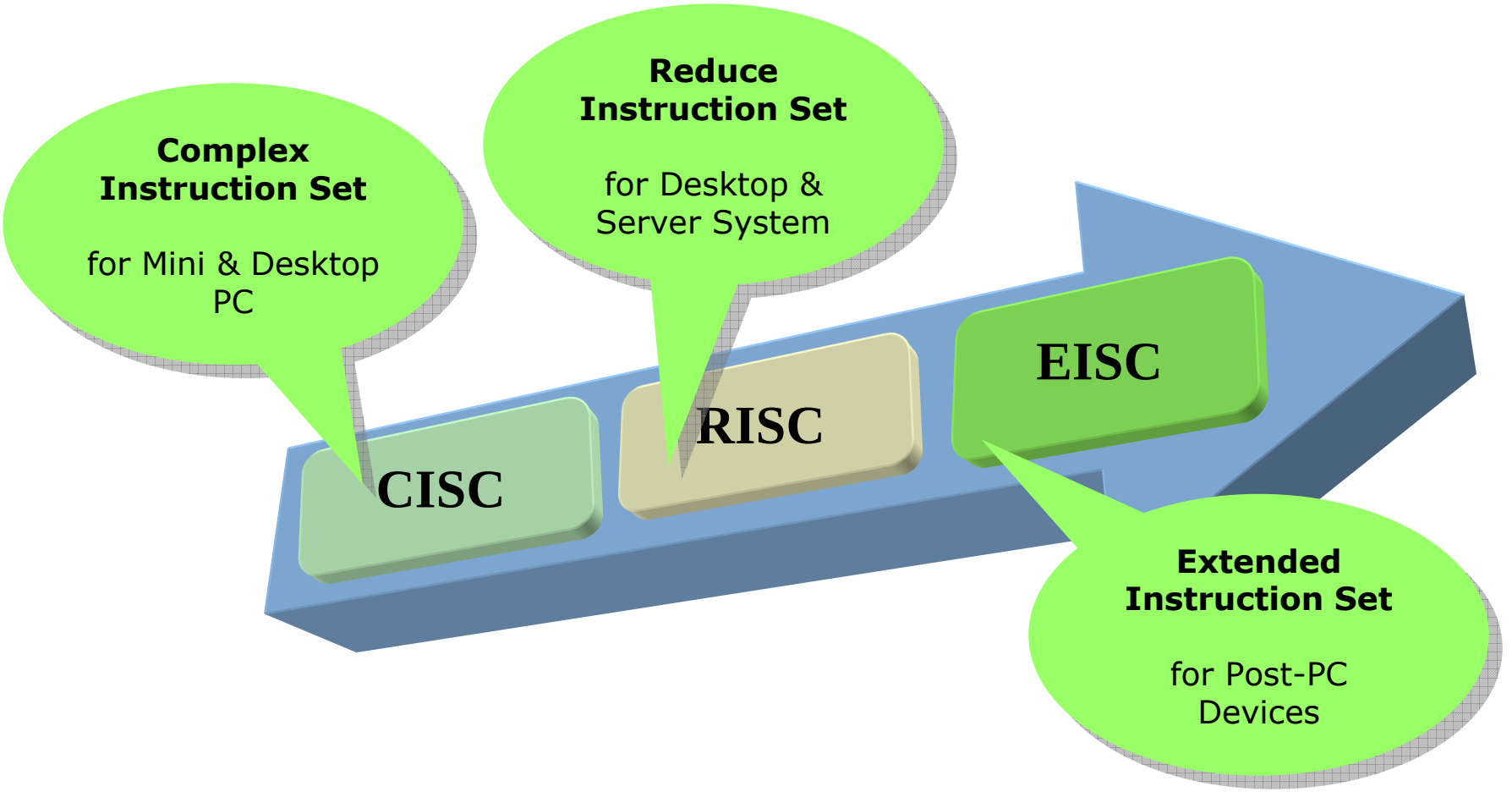
EISC (Extendable Instruction Set Computer) is a new ISA (Instruction Set Architecture) and computer architecture developed by ADC (Advanced Digital Chips Inc).

it combines key advantages of two leading architectures: Reduced Instruction Set Computer (or RISC) and Complex Instruction Set Computer (or CISC)



Microprocessor

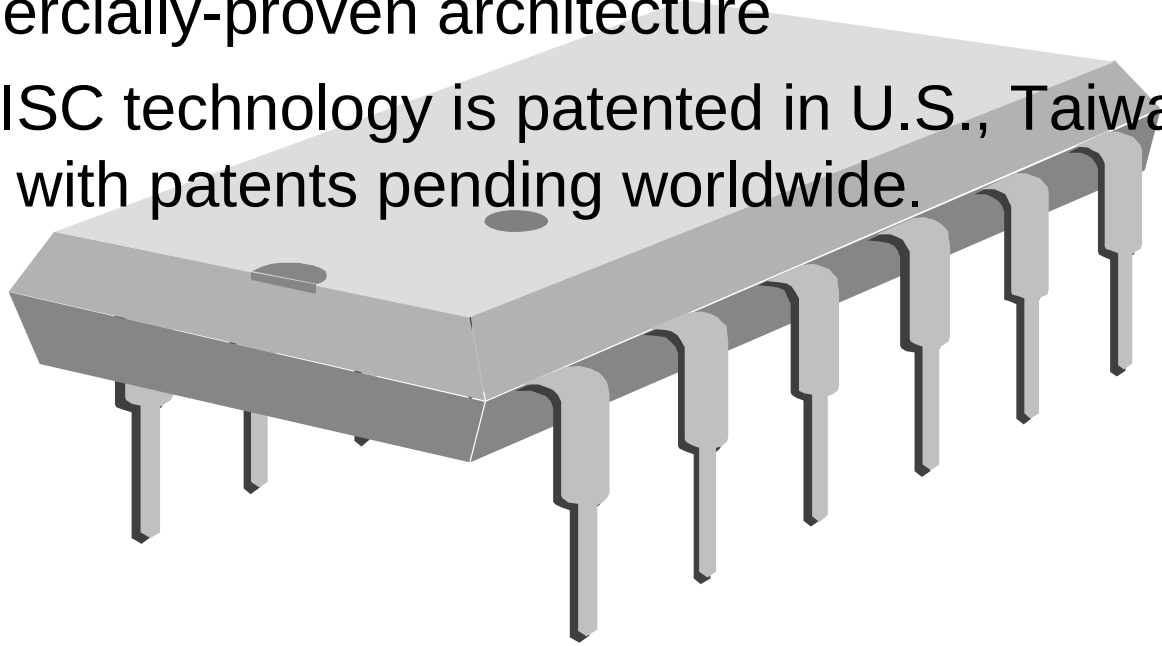
- Development Cycle in Microprocessor



EISC is a next generation architecture that has advantages over the existing RISC and CISC architectures.

next generation Microprocessor EISC

- ADC is the only house with own its proprietary commercially-proven architecture
- The EISC technology is patented in U.S., Taiwan and Korea with patents pending worldwide.



Bench mark Results

	AE32000	SE3208	ARM7TDMI	MIPS-R3000
Technology	0.5um	0.5um CMOS	0.5um(0.35um)	0.5um CMOS
Clock Frequency	50Mhz	50Mhz@5V	33Mhz(55Mhz)	
Code Size	100	-	100	177.7
Gate count	34K	20K	42K	-
Power consumption		200mW	330mW(0.6mw/Mhz)	-
Chip size		1000x1000(target)	1892x1168	-
Performance	0.8	0.634	0.7	

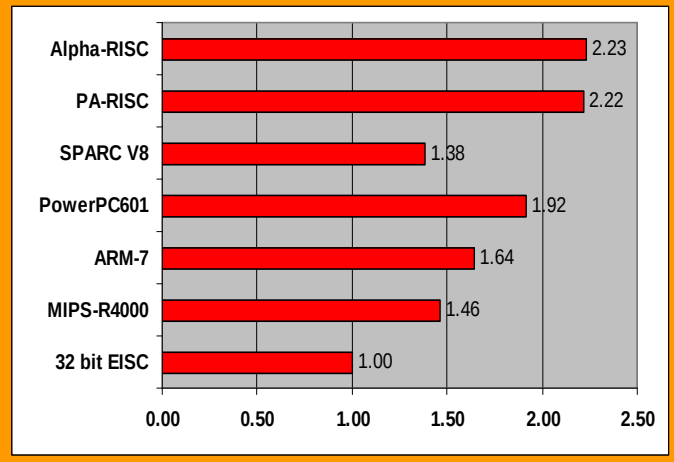
* Better core density
* Simple Instruction set
* Smaller silicon (half that of ARM) die size, hence,cheaper.
* "Extendible"=more flexible

EISC benefits

Technology Advantage - Comparison

	CISC	RISC	EISC
Major Features	- for high-end computers	- 32-bit fixed code	- Post-PC Devices - Scalable = 16, 32, 64 Bit Solutions
Code Instruction	Complex	Simple	Simple
Relative Program Size	130-140	160-180	100
Performance	Low	High	High
Embedded	Not Suitable	High	Ideal
Weaknesses	- Complex code and hardware - Difficult to develop-high-end MCU (64-bit and higher)	- Difficult to develop 16-bit MCU - Not efficient for 64bit MCU	

Source : Company Data



Advantage of both CISC and RISC
1.Simple Instruction Set
2.Less Memory
3.Simple Hardware
4.Less Power

Lower Development Cost
Faster Time to Market
Higher Performance / $

Embedded MCU Soft core IP

SE 1608	SE 3208	AE 32000 B/C	AE 64000
▪ 16 bit ALU/Data/Address ▪ 64K byte address ▪ 60MHz@0.35um ▪ 8K Gate Count	▪ 32 bit ALU/Data/Address ▪ 4G byte address ▪ 60MHz@0.35um ▪ 24K Gate Count	▪ 32 bit ALU/Data/Address ▪ 4G byte address ▪ DSP ▪ FPU ▪ 120~150 MHz @0.18um ▪ 46K Gate Count	▪ 64 bit ALU/Data/Address ▪ 4T byte address ▪ FPU ▪ SIMD-DSP ▪ 100 MHz@0.18um ▪ 140K Gate Count
8GPR/6SPR, 3 Stage Pipeline		16GPR/7SPR, 5 Stage Pipeline, MMU, Harvard Architecture 4 Co-Processors	
BPR for Debug	On-Chip Debugger(On Silicon ICE)		
Load-Store Instruction Set			
16 bit Fixed Length Instruction Set & Extendable Instruction Set(LERI)			

IP LIST

Microprocessor
❖ 16bit EISC Microprocessor - SE1608A
❖ 32bit EISC Microprocessor - SE3208A
❖ 32bit EISC Microprocessor - AE32000B
❖ 64bit EISC Microprocessor – AE64000
❖ 64bit SIMD/DSP
❖ 64bit FPU
❖ Unified Cache Controller
❖ Harvard Cache Controller (TLB)
❖ Memory Management Unit
❖ Low power Cache Controller

H.264 CODEC/ JPEG CODEC
❖ H.264 encoder/decoder
❖ MJPEG encoder/decoder

IP LIST

Special Peripherals		
ADPCM	ADPCM Decoding Engine (CCITT G.726)	
Bit Block Transfer controller	Screen to screen block transfer & sprite	
Sound Engine	32 channel, 16bit, ~44.1㎑ stereo PCM, 8bit, U-Law/PCM, 16bit PCM	
2D Graphic based on 3D	Rotation/Zoo In-out Texture and Tile map Transparency, Alpha Blending	
Video Encoder	Hue Program Control, RGB to YCbCr Converter Programmable C-Filter Bandwidth Programmable Multi-Standard Format	

Peripherals		
B-INTC	Basic Interrupt Controller	
B-TIMER	Basic Timer	
SMC	Static Memory Controller	
GDMAC	General DMA Controller	
UART	Universal Asynchronous Receiver/Transmitter	

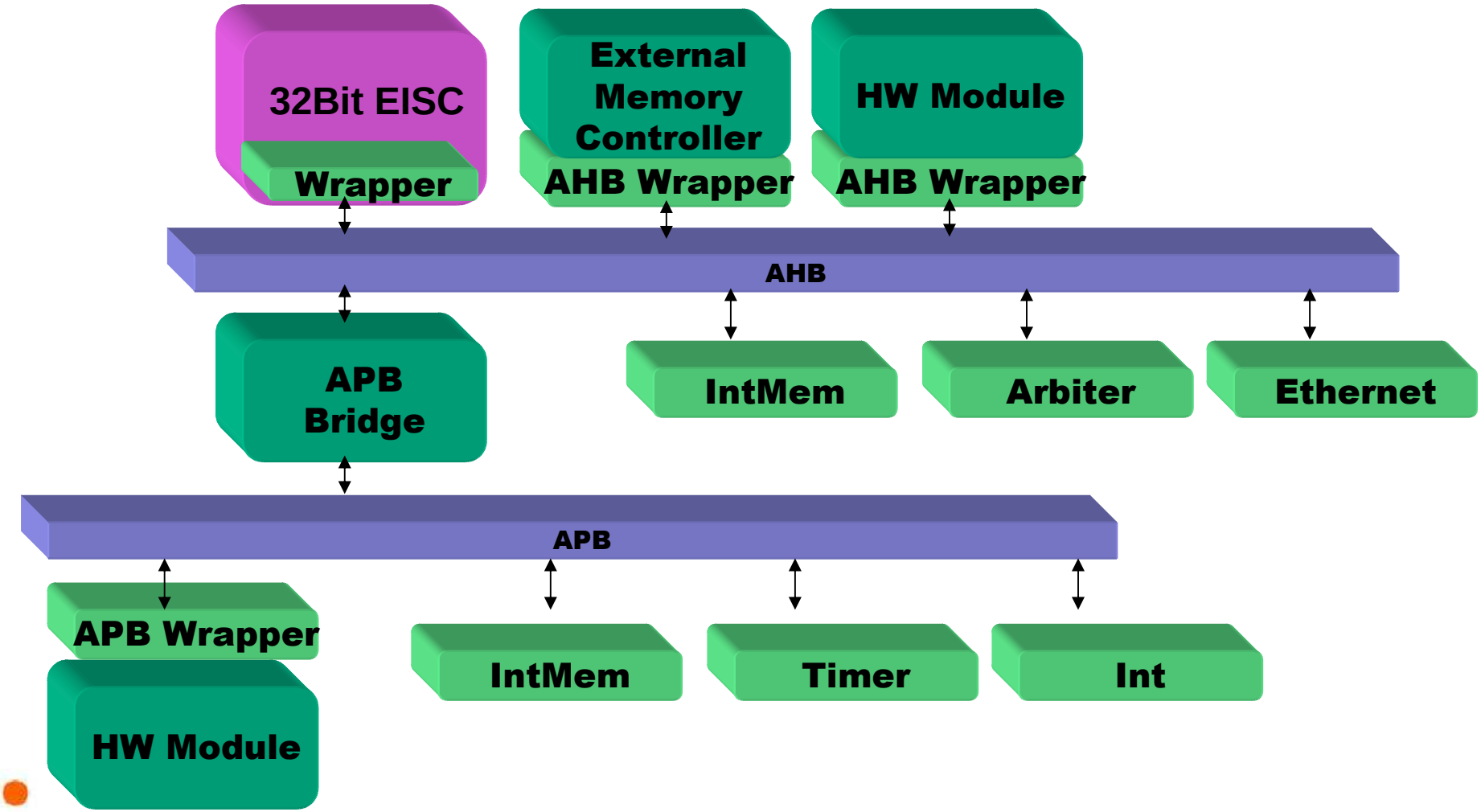
IP LIST

Peripherals		
PWM	Pulse Width Modulation	
PPM	Pulse Period Measurement	
I2C	Inter IC Bus Controller	
I2S	Inter IC Sound Bus Controller	
WDT	Watch Doc Timer	
GPIO	General Purpose Input Output Controller	
PINTC	Priority Programmable Interrupt Controller	
SIO	Sync. IO Bus Controller	
RTC	Real Time Clock	
Key Scan	Key Input Scan Controller	
SPI	Serial Peripheral Interface Controller	
HDLC	High Level Data Link Controller	

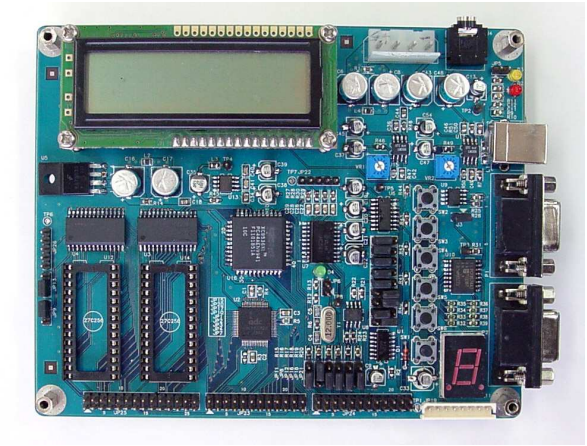
Peripherals		
IEEE1284-Host	Parallel Bus Master Controller	
IEEE1284-Device	Parallel Bus Slave Controller	
NOR-FMC	Nor Type Flash Memory Controller	
NAND-FMC	Nand Type Flash Memory Controller	
PCMCIA	PCMCIA Host Bus Adapter	
IDE	IDE Controller for HDD Interface	
LCDC	Mono/STN LCD Controller	

SoC Platform

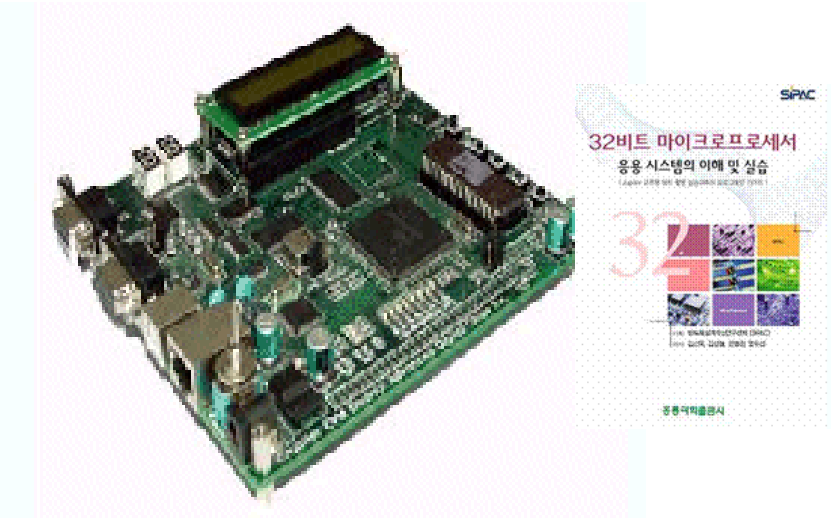
Platform embodiment based on AMBA/AHB



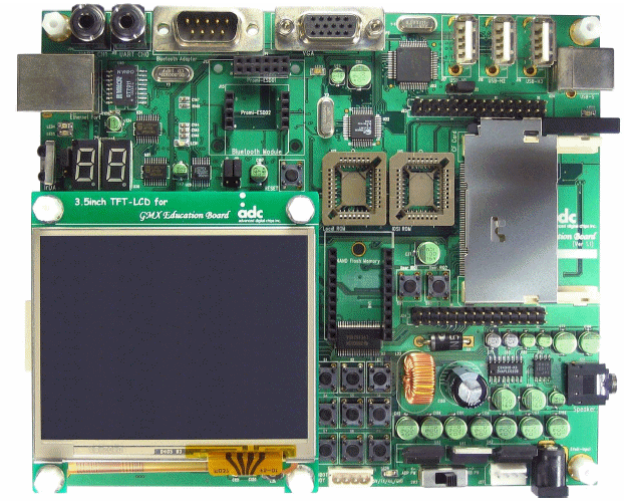
EISC EVM Board



1) 16Bit Embedded Board (16S310)



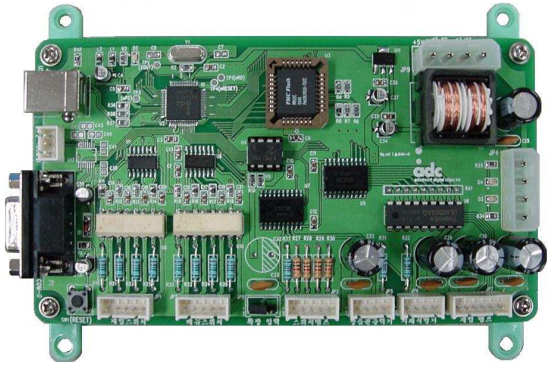
2) 32Bit Training Board (Jupiter)



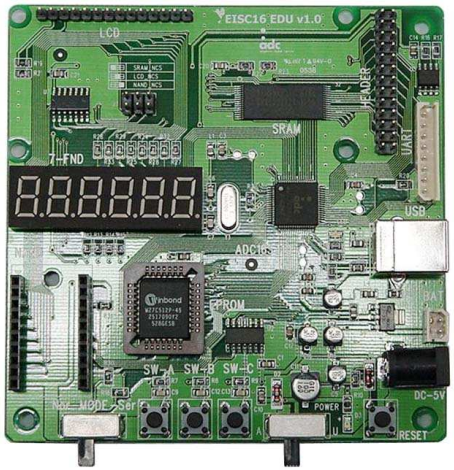
3) 32Bit Training Board (GMX1000)

4) 32Bit Game Board (Amazon)

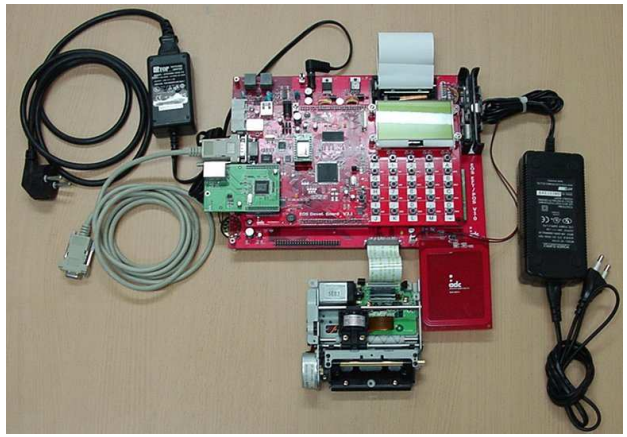
EISC EVM Board



1) I/O Control board for Game

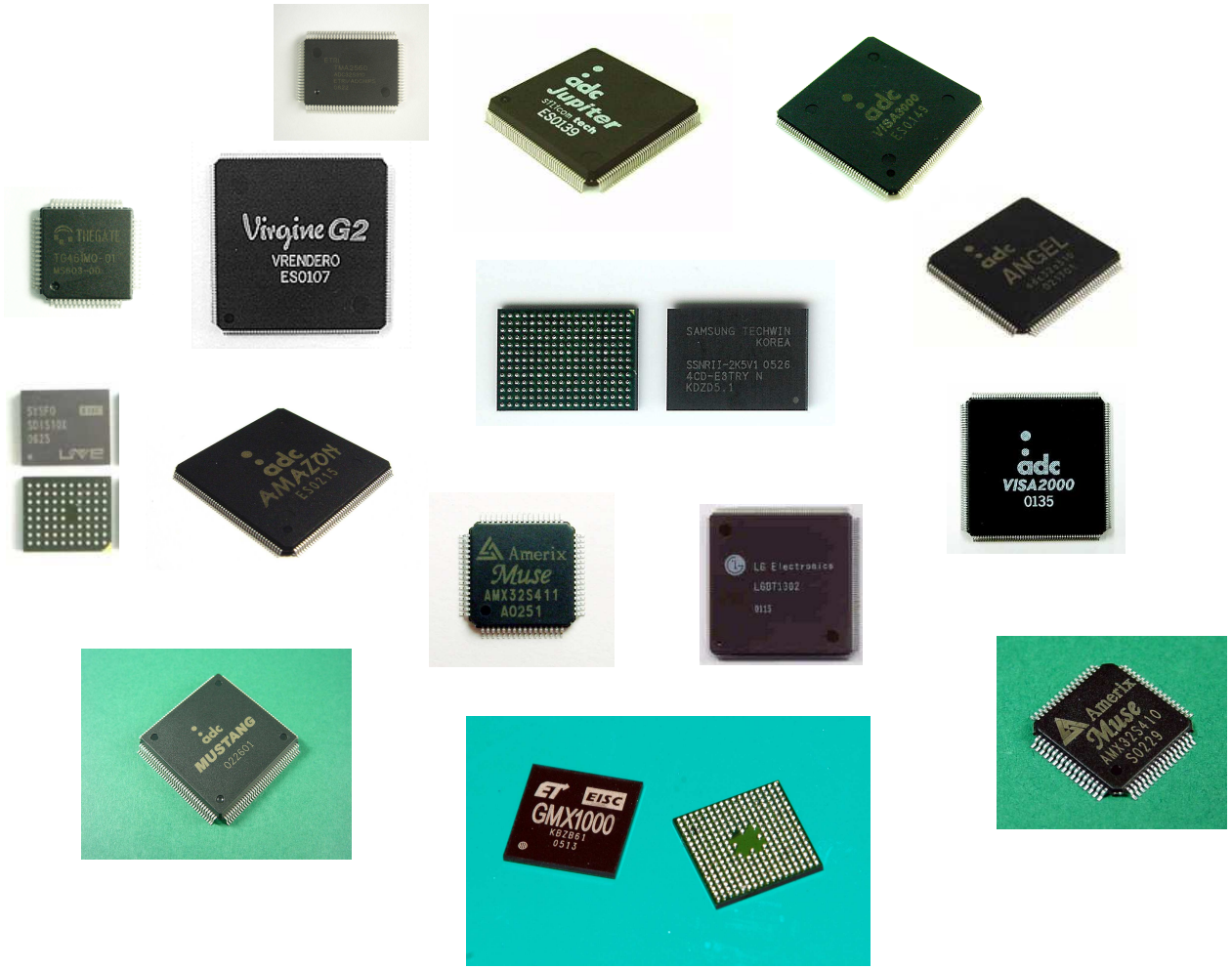


2) 16bit Training Kit



3) 32bitEFT/POS Terminal board (eos)

ADC's SoC Productions



Partnership EISC's key strength

EISC

SAMSUNG TECHWIN

LG Electronics

DongbuAnam Semiconductor

MCWILL

dynalith

PLANET
THE POWER LINE ADVANCED NETWORK

Sysfo Lab.

UNIANA
www.uniana.com

ENTER

namco

株式會社자티電子

KDE

adc

EISC

한국전자통신연구원

STA

Swip

AMERIX CORPORATION

ADCUS,INC.

서울대학교 SEOUL NATIONAL UNIVERSITY

KAIST

연세대학교 YONSEI UNIVERSITY

고려대학교

한국정보통신대학교 Information and Communications University

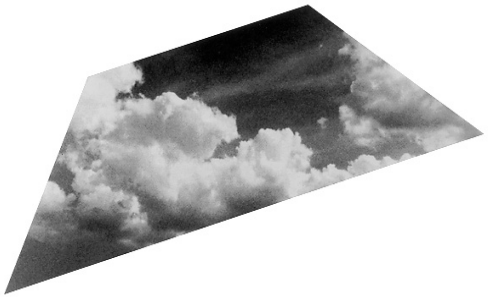
광주과학기술원

경희대학교 Kyung Hee University

한양대학교 HANYANG UNIVERSITY

SoC Successful Story

(Reference Story)



EISC is a proven technology

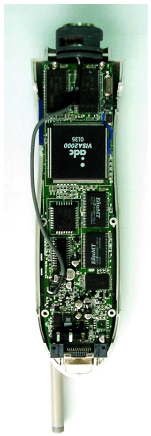
adc

Ⅰ. Reference Story

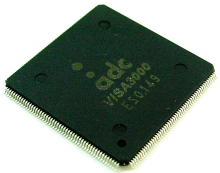
VISA 2000

1. KORITECH

-. Being applied to the handy Karaoke
-. A strategic product for overseas Market



VISA 3000



1. Enter-Tech

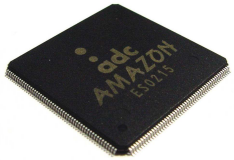
-. Being applied to the handy Karaoke
-. Overseas export product

Ⅰ. Reference Story

EISC

VirgineG2

AMAZON



1. NAMCO (in Japan)

NAMCO GROUP WORLDWIDE

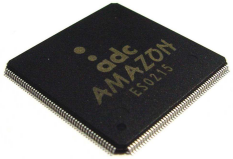
-. Being applied to the gambling game
-. Being applied to the arcade game
-. Apply to the AMAZON

2. Para Enterprise -. Arcade Game / Gambling Game

adc

Ⅰ. Reference Story

AMAZON



1. VISCO (in Japan) -. Arcade Game / Gambling Game

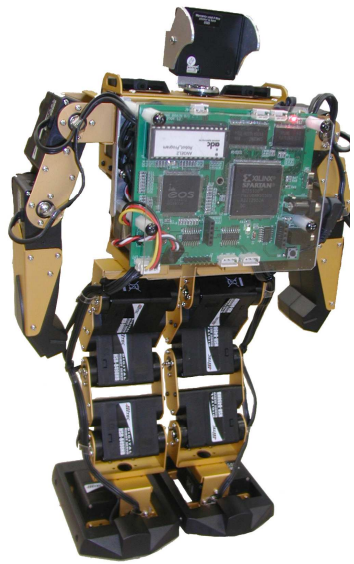
2. UNIANA -. Arcade Game

Ⅰ. Reference Story

Jupiter

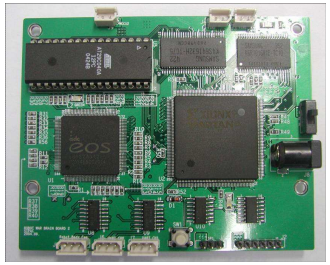
eos

5’rd SoC RobotWar competition hold with EISC CPU brain board at AP SoC (Asia pacific on Chip) 2006.



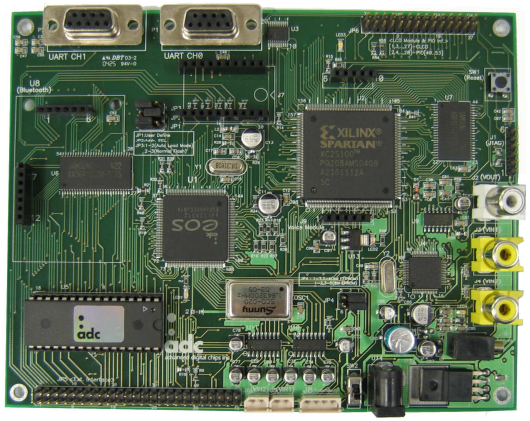
adc

SoC Taekwon Robot board

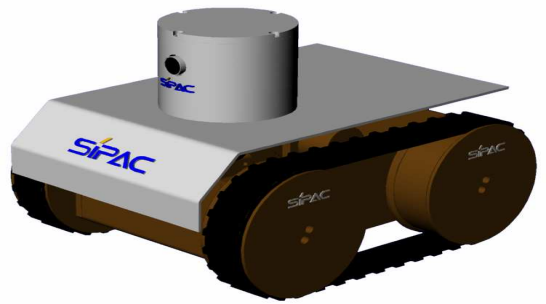


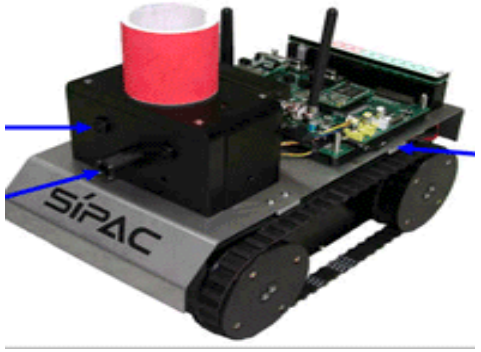
1) Taekwon Robot board

SoC TANK Robot Board



2) Tank Robot Brain Board





Training Kit

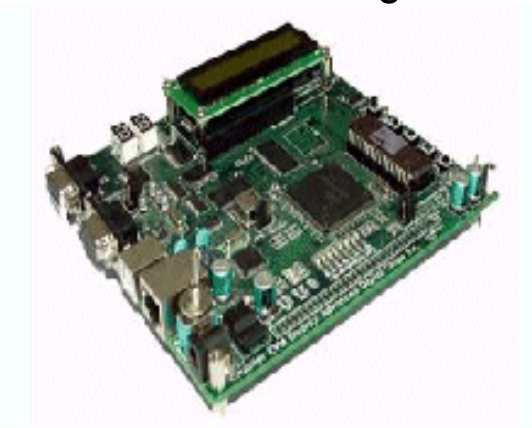
Jupiter

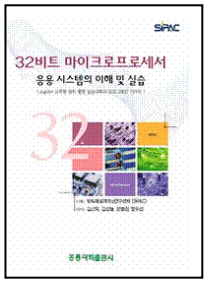
- **Educational Training Kit for 32bit embedded system and S/W**

Training Book

Jupiter

- **Educational Training Kit for 32bit embedded system and S/W**

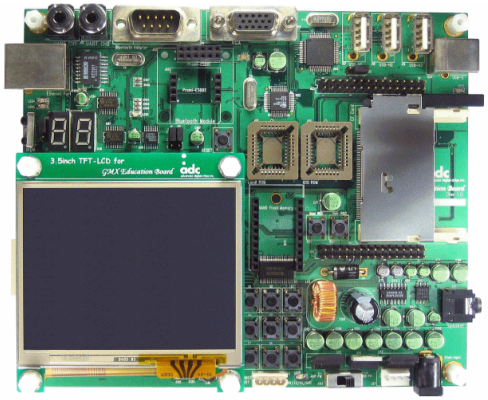




Training Book

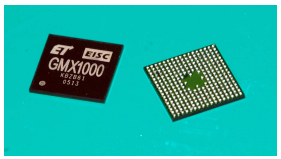
Training Kit

GMX1000 training board



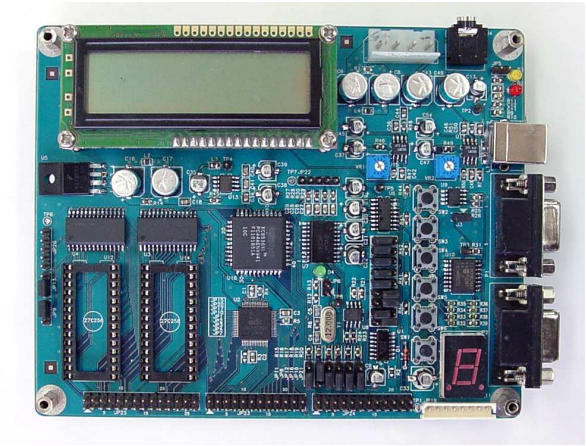
GMX1000 training kit

3D animation training board

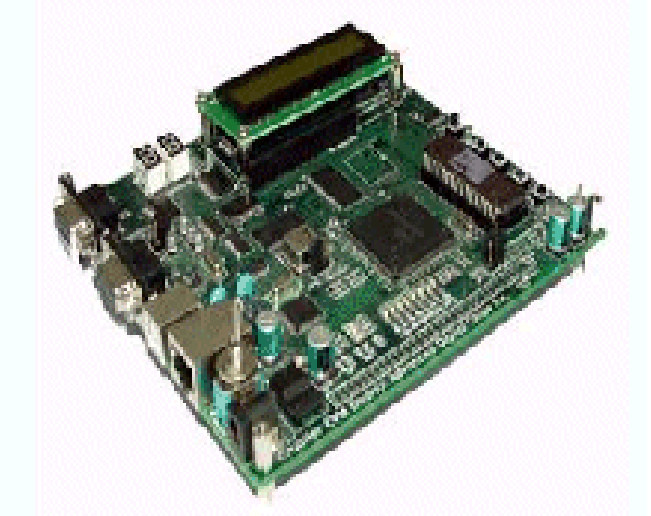


3D animation training kit

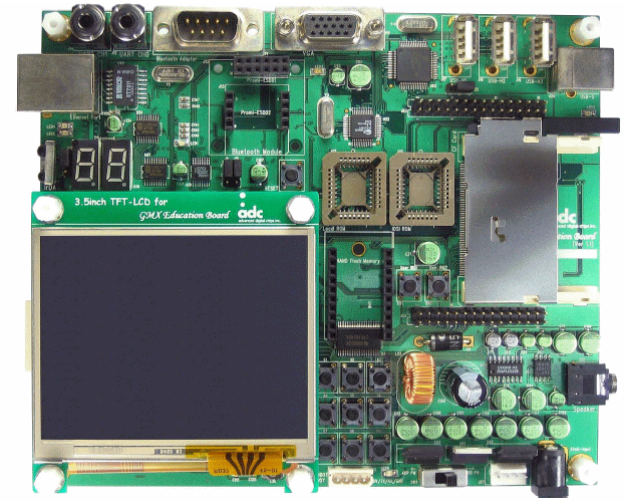
EISC EVM Board



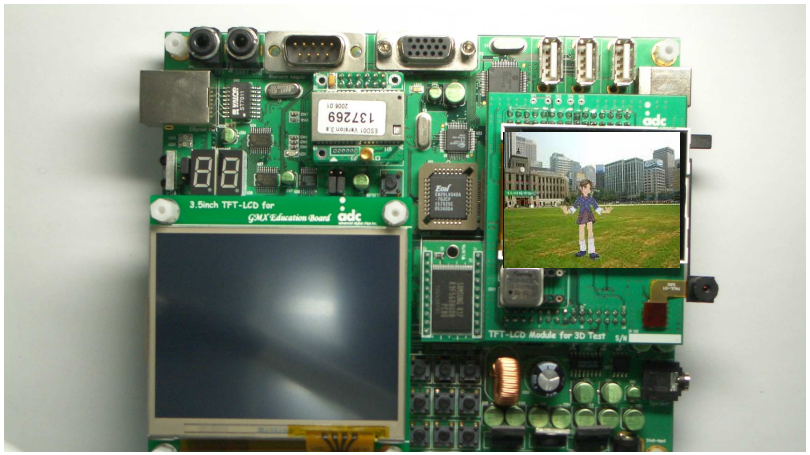
1) 16Bit Embedded Board (16S310)



2) 32Bit Training Board (Jupiter)

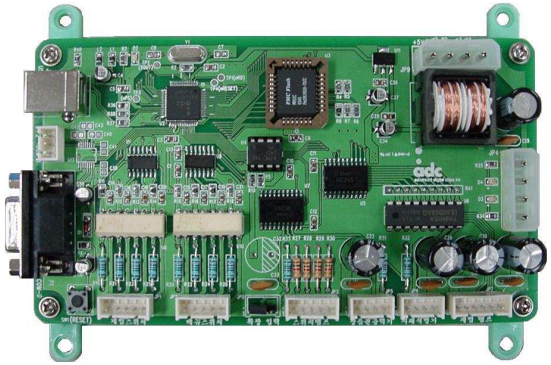


3) 32Bit Training Board (GMX1000)



4) 32Bit 3D Game Training Board (Amazon)

EISC EVM Board



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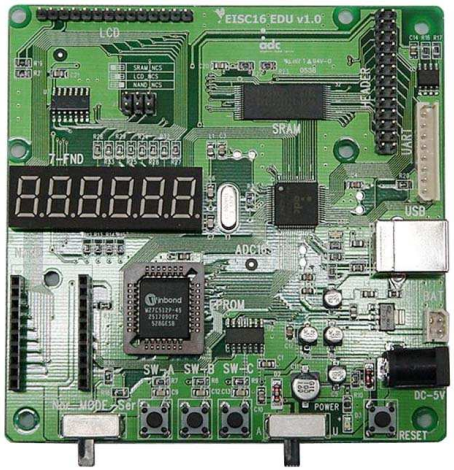
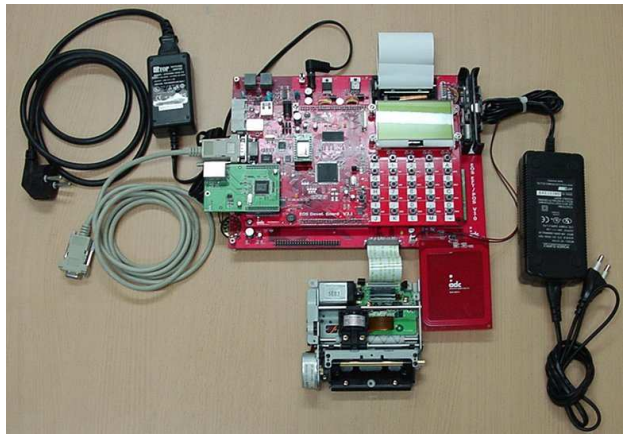


2) 16bit Training Kit



3) 32bitEFT/POS Terminal board (eos)

4) 32Bit Game Board (Amazon)

Ⅰ. Reference Story

STA (Australia)

LG Electronic

License contract signed with STA in Australia.(2000.9)

Developed the Power Line Communication System Solution chip
Powerful Power Line Transceiver and control networking protocol firmware into a single ch

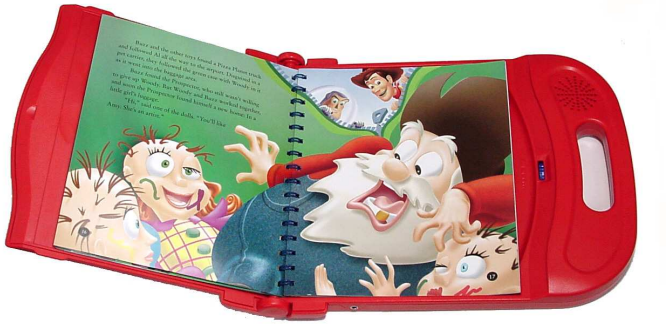
License contract signed on 32bit EISC with LG Electronics (1999.11)

Developed Digital TV chip set

Ⅰ. Reference Story

Muse2

1. ADPCM chip
   - -. Being applied to the Saying book
   - -. Being applied to the Talking Dog



Ⅰ. Reference Story

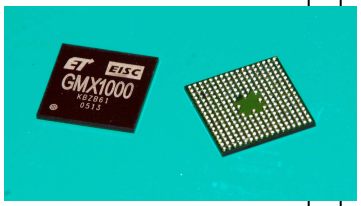
Muse2

Being applied GPS Appliance

GUGU Toy (www.구구토이.co.kr)

Ⅰ. Reference Story

GMX1000



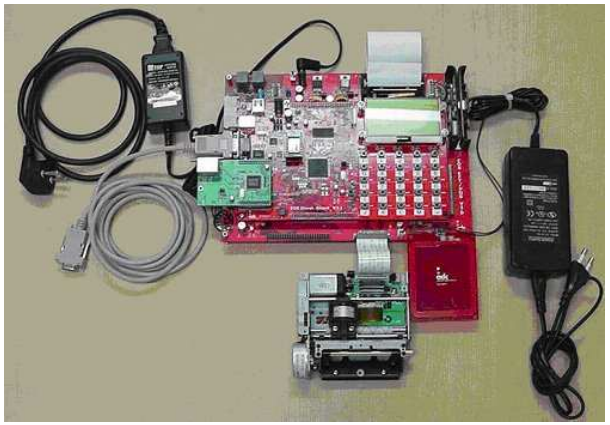
Multimedia processor

-. Being applied to the handy Karaoke, Game and etc.

Ⅰ. Reference Story

eos

Being applied to EFT/POS & PINPAD Appliance



SE16S310

USB controller with 16bit CPU.

Ⅰ. Reference Story

Mewtel

www.mewtel.com

Under develop

License contract signed with Metel (2004)

Under developing wireless chip set for MP3 and mobile phone.

Ⅰ. Reference Story

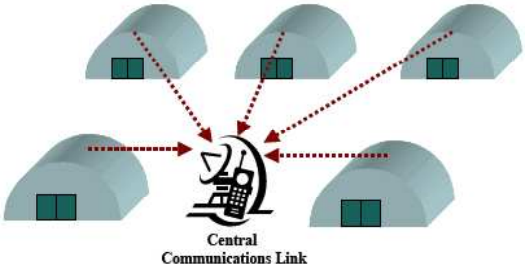
TMA2560

ETRI 국책 과제

Under developing Active RFID reader processor

- Secured cargo visibility

- military



- Waterpark safety

safetzone

SafeTzone Technology Corporation
22941 Mill Creek Road
Laguna Hills, CA 92653
Phone: 949.855.8987 ● Fax: 949.855.3709
www.safetzone.com

Guests simply swipe their wristbands over the LocationStation's reader to display the real-time location of each group member.

Ⅰ. Reference Story

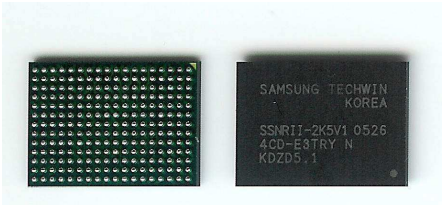
Winner3

SamSung Techwin & Sysfolap

License contract signed with SamSung Techwin (2005)

Being applied to high resolution CCTV camera

High resolution Day&night DSP chip



Winner4

SamSung Techwin & Sysfolap

Under developing Winner4 Project

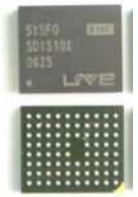
Being applied to high resolution camera for car

High resolution Day&night DSP chip

Ⅰ. Reference Story

SDIS

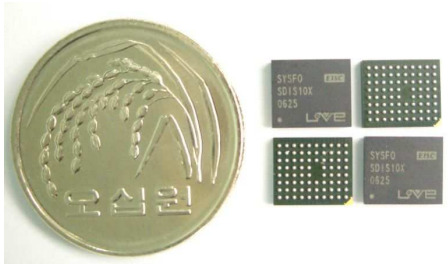
(sysfo lap)



EYENIX

SAMSUNG
TECHWIN
Under develop
(sysfo lap)

3M pixel mobile camera phone chip
Being applied mobile camera phone.



CMOS/CCD
이미지 센서

Under developing 5M pixel mobile camera phone chip)

Ⅰ. Reference Story

DMB decoder

Under develop

Under developing DMB multimedia processor

Ⅰ. Reference Story

TG461

Mixed microprocessor with OP amp

Writing with supersonic wave's pen.

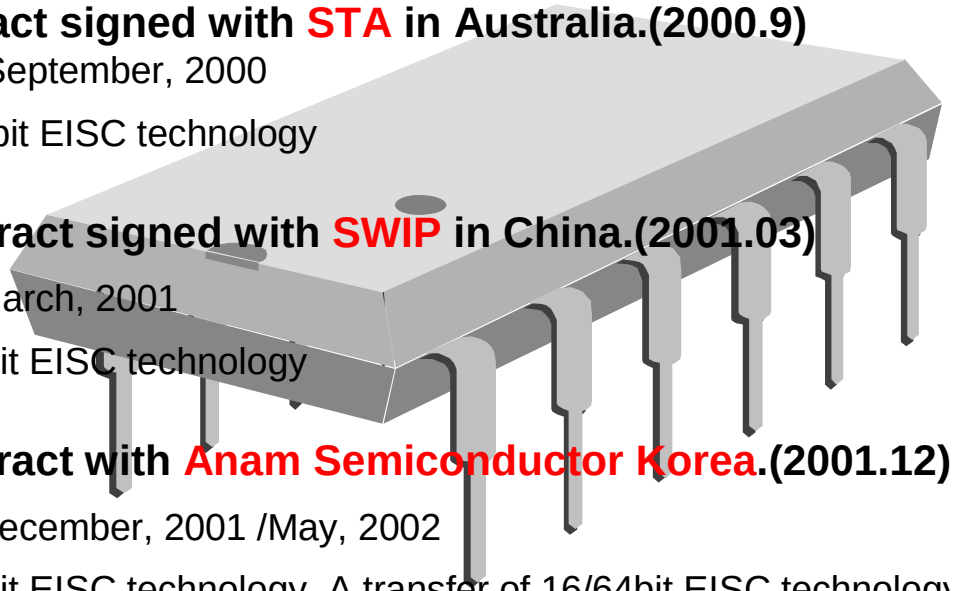
Ⅱ. IP License Contract

1. License contract signed on 32bit EISC with LG Electronics (1999.11)

- Effective date: November, 2001
- A transfer of 32bit EISC technology

2. License contract signed with STA in Australia.(2000.9)

- Effective date: September, 2000
- A transfer of 32bit EISC technology



3. Licensed contract signed with SWIP in China.(2001.03)

- Effective date: March, 2001
- A transfer of 16bit EISC technology

4. Licensed contract with Anam Semiconductor Korea.(2001.12)

- Effective date: December, 2001 /May, 2002
- A transfer of 32bit EISC technology, A transfer of 16/64bit EISC technology

5. Licensed contract with Amerix group in U.S.A (2002.3)

- Effective date: March, 2002
- A transfer of 16/32/64bit EISC technology (Allowance of master license)

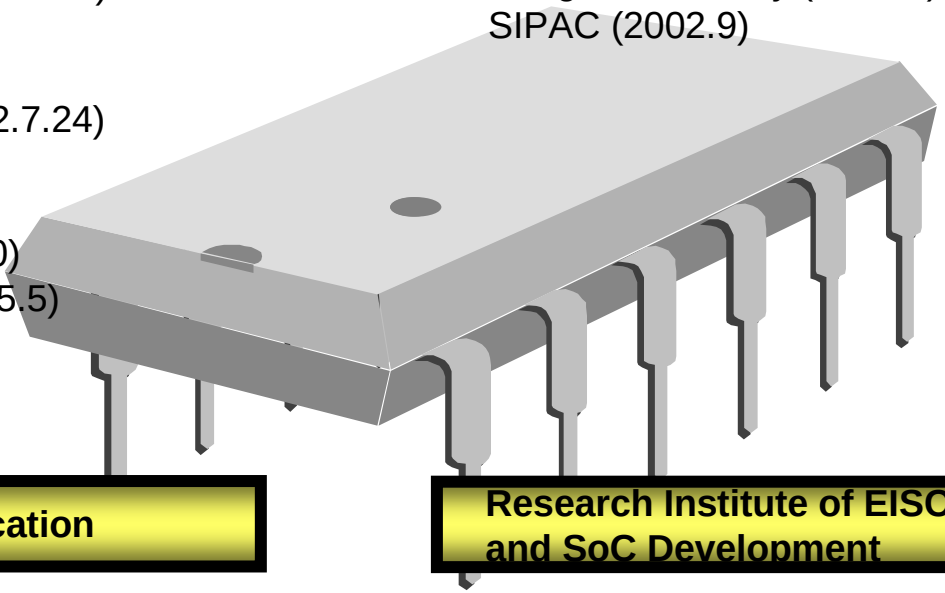
III. Other Activities

Contribute EISC CPU to the university

Seoul Nat'l University (2002.5.7)
KAIST (2002. 6.27)
ICU (2002.6.27)
Kyunghee University(2002.7.24)
KJIST (2003.3)
Korea University(2003.9)
Yunsei University(2003.10)
HanYankg University(2005.5)

Contribute evaluation board to the university

Hong Ik University (2003.5)
SIPAC (2002.9)



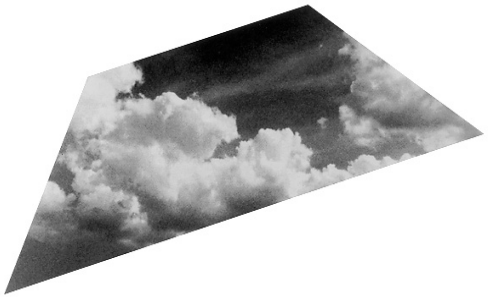
EISC Cooperative Education

Korea Univ. (Professor Oh.)
Korea Univ. (Professor Choi.)
Yunsei Univ. (Professor Lee.)
BuKyung Univ. (Professor Cho.)
Oregon state Univ. (Professor Ben Lee)
Cheju National Univ.(Professor Lim)

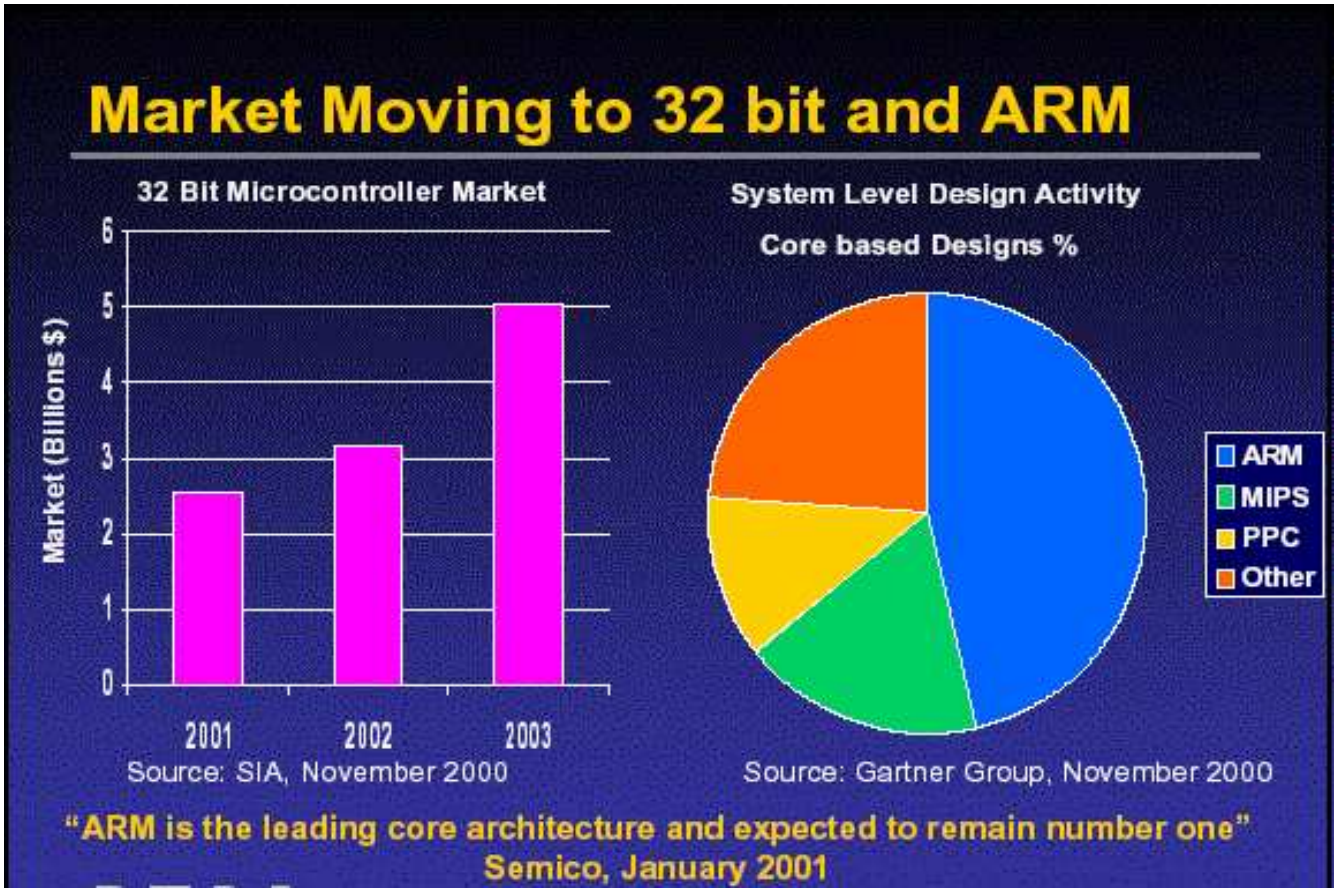
Research Institute of EISC Platform and SoC Development

ETRI (Manager Cho)
KAIST SIPAC (Professor Yu)
ICU (Professor Park)

EISC Tech. Bechmarking & Biz. Strategy



Embedded Microprocessor Market



Comparison Table

Comparison of ARM7 with SE3208

	SE3208(Jupiter)	ARM7TDMI	MIPS-R3000
Technology	0.35 um CMOS	0.35 um CMOS	0.35 um CMOS
Clock Frequency	60Mhz @ 3.3V	55Mhz	
Code Size	100	113.9(ARM7:165)	166.7
Gate count	24K	42K	?
Power consumption	300 mW(target)	330mW (0.6mw/Mhz)	?
Chip size	1000x1000(target)	1829x1168	?

Clock frequency can be improved by customizing the cache block.

Comparison of i8051 and Z80 with SE1608

	SE1608(16bit)	i8051 (8bit MCU)	Z80 (8bit MCU)
Gate count	4~6K	8K	10K
Architecture	RISC Type	CISC Type	CISC Type

Comparison Table

Comparison of ARM9 with AE32000

	ARM920T	AE32000(Angel)	Remark
Code Size	?	Good	
IPC	0.67(ARM7=0.53)	0.87	Based on Dhrystone 2.1
Pipeline	5 stage pipeline	5 stage pipeline	
Cache	Harvard architecture	Harvard architecture	
MMU	Support	Support	
Performance	200MHZ(0.18μ)	120MHZ(0.18μ) (not optimize of cache block Layout)	
Area	2,500K Tr.	1,348K Tr.	

Comparison Table

Comparison of Code Size

	AE32000	Mips-r3000	ARM7TDMI
Relative Code Density	100	171	110

SH-3(Hitachi)	130
V850(NEC)	118
MC5200(Motorola)	139(coldfire)

Platform : Linux (Window-95/98, Window-NT)

Compiler : GCC-2.95.2 (FSF GNU GCC)

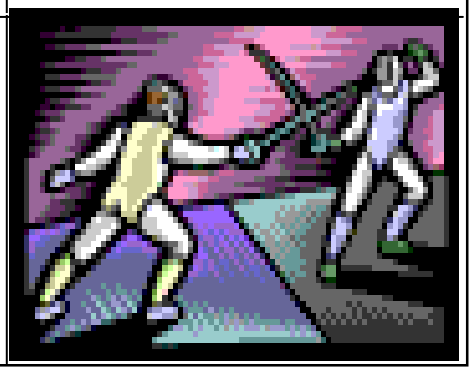
Object Program : ANSI C library programmed by Cygnus

C Math library programmed by Sun used at Sun workstation

C++ Standard Template Library by SGI used at SGI workstation

Compiled machine code size : 381,560 bytes at MIPS-R3000

Technology Advantage - Comparison

	CISC	RISC	EISC
Major Features	- for high-end computers	- 32-bit fixed code	- Post-PC Devices - Scalable = 16, 32, 64 Bit Solutions
Code Instruction	Complex	Simple	Simple
Relative Program Size	130-140	160-180	100
Performance	Low	High	High
Embedded	Not Suitable	High	Ideal
Weaknesses	- Complex code and hardware - Difficult to develop-high-end MCU (64-bit and higher)	- Difficult to develop 16-bit MCU - Not efficient for 64bit MCU	

Source : Company Data

Strategy for overcoming the ARM market

Marketing Strategy of EISC CPU

1) Free offer and open to the public of compiler, development environment, source code of RTOS

2) The supply of 32bit EISC CPU board for education (Use for education of university and institute)

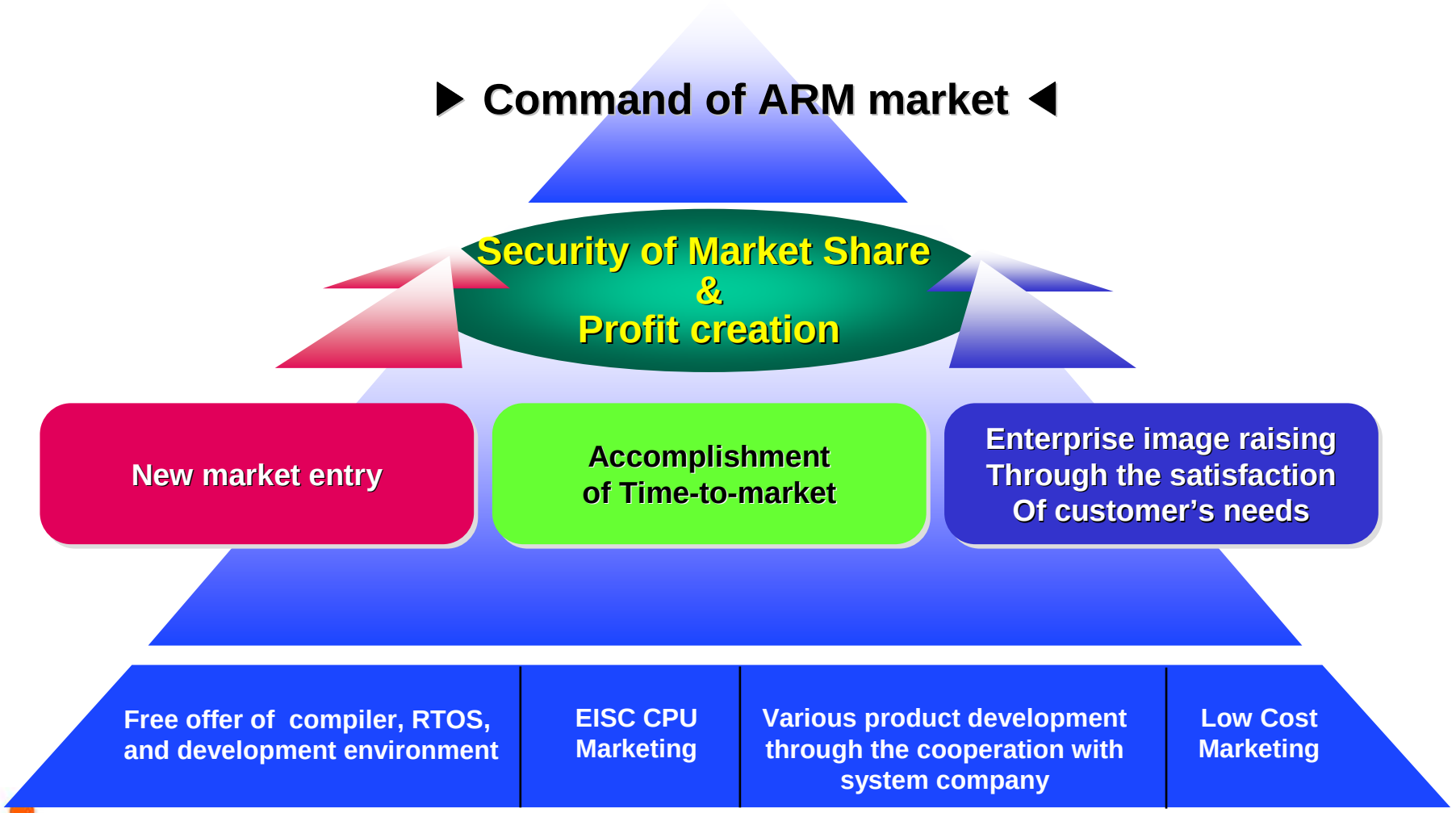
3) The open to the public of embedded Linux

4) Open a competitive exhibition which is included the robot football and robot war, and grant of premium and prize for the winning team

5) The joint ownership of technology through the organization of EISC CPU group

Strategy for overcoming the ARM market

(Image Making)



Thank you…