Solutions to Problems Marked with a * in
Logic and Computer Design Fundamentals, 4th Edition

Chapter 11

11-2.*

a) The latency time = 0.5 ns x 8 = 4.0 ns.

b) The maximum throughput is 1 instruction per cycle or 2 billion instructions per second.

c) The time required to execute is 10 instruction + 8 pipe stages -1 = 17 cycles *0.5ns = 8.5ns

11-6.*

Cycle 1: PC = 10F

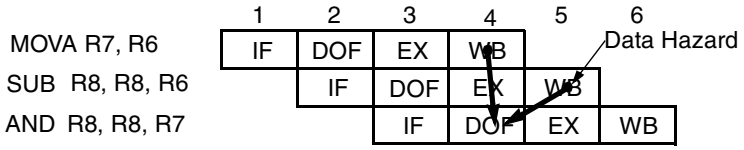
Cycle 2: PC_{-1} = 110, IR = 4418 $2F01_{16}$

Cycle 3: PC_{-2} = 110, RW = 1, DA = 01, MD = 0, BS = 0, PS = X, MW = 0, FS = 2, SH = 01, MA = 0, MB = 1
BUS A = 0000 001F, BUS B = 0000 2F01

Cycle 4: RW = 1, DA = 01, MD = 0, D0 = 0000 2F20, D1 = XXXX XXXX, D2 = 0000 00000

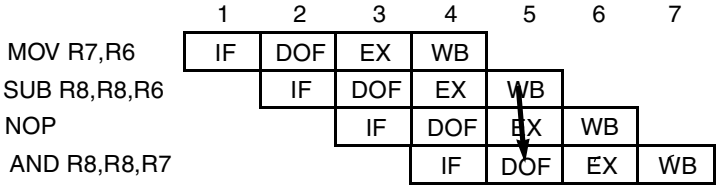
Cycle 5: R1 = 0000 2F20

11-10.*

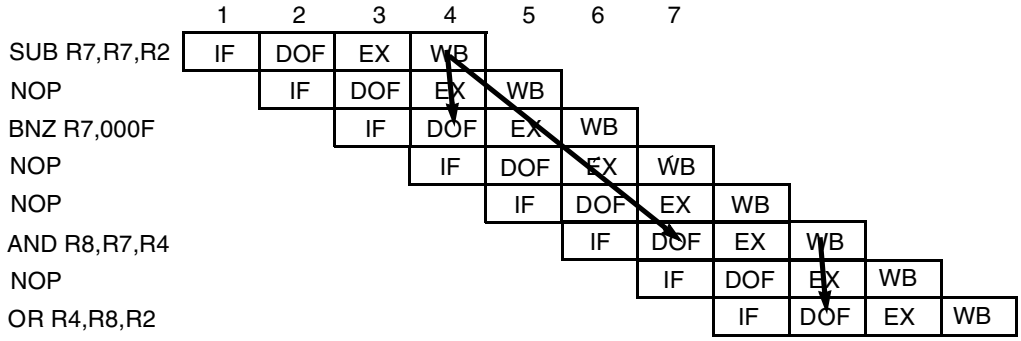


11-12.*

a)



b)



11-15.*

Time Cycle 1

IF PC: 0000 0001
DOF PC_{-1}:XXXXXXXX IR: XXXXXXXX
EX PC_{-2}:XXXXXXXX A: XXXXXXXX B: XXXXXXXX RW:X DA:XX MD:X BS:X PS:X MW:X FS:X MB:X MA:X CS:X D':X
WB D0: XXXXXXXX D1:XXXXXXXX D2:XXXXXXXX RW:X DA:XX MD:X

Time Cycle 2

IF PC: 0000 0002
DOF PC_{-1}:0000 0002 IR: 0A73 8800
EX PC_{-2}:XXXXXXXX A: XXXXXXXX B: XXXXXXXX RW:X DA:XX MD:X BS:X PS:X MW:X FS:X MB:X MA:X CS:X D':X
WB D0: XXXXXXXX D1:XXXXXXXX D2:XXXXXXXX RW:X DA:XX MD:X

Time Cycle 3

IF PC: 0000 0003
DOF PC_{-1}:0000 0003 IR: 9003 800F
EX PC_{-2}:0000 0002 A: 0000 0030 B: 0000 0010 RW:1 DA:07 MD:0 BS:0 PS:X MW:0 FS:5 MB:0 MA:0 CS:X D':X
WB D0: XXXXXXXX D1:XXXXXXXX D2:XXXXXXXX RW:X DA:XX MD:X

Time Cycle 4

IF PC: 0000 0004
DOF PC_{-1}:0000 0004 IR:1083 9000
EX PC_{-2}:0000 0003 A: 0000 0020 B: XXXXXXXX RW:0 DA:XX MD:X BS:1 PS:1 MW:0 FS:0 MB:1 MA:2 CS:1 D':1
WB D0: 0000 0020 D1:XXXX XXXX D2:0000 0000 RW:1 DA:07 MD: 0 PC: 0000 0012

Time Cycle 5

IF PC: 0000 0013 R7: 0000 0020
DOF PC_{-1}: 0000 00013 IR: 1244 0800
EX PC_{-2}: 0000 0004 A: 0000 0020 B: 0000 0020 RW: 1 DA: 08 MD: 0 BS: 0 PS: X MW: 0 FS: 8 MB:0 MA:0 CS:X D':X
WB D0: 0000 0020 D1: XXXXXXXX D2: 0000 0000 RW: 0 DA: 00 MD: 0

Time Cycle 6

IF PC: 0000 0014
DOF PC_{-1}: 0000 0014 IR: XXXX XXXX
EX PC_{-2}: 0000 0013 A: 0000 0020 B: 0000 0010 RW: 1 DA: 04 MD: 0 BS: 0 PS: X MW: 0 FS: 9 MB:0 MA:0 CS:X D':X
WB D0: 0000 0010 D1: XXXX XXXX D2: 0000 0000 RW: 1 DA: 08 MD: 0

Time Cycle 7

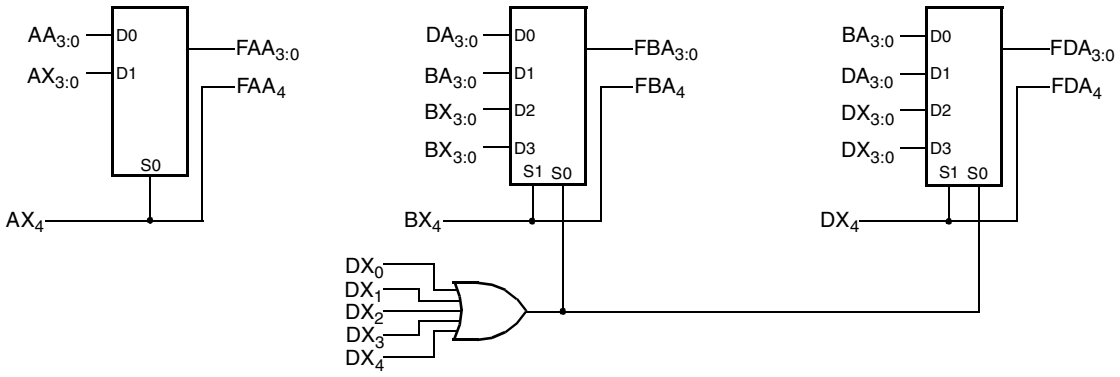
IF PC: 0000 0014 R7: 0000 0020
DOF PC_{-1}: 0000 0014 IR: XXXX XXXX
EX PC_{-2}: 0000 0013 A:XXXX XXXX B: XXXX XXXX RW: X DA: XX MD:X BS: X PS:X MW:X FS:X MB:X CS:X D':X
WB D0: 0000 0010 D1: XXXX XXXX D2: 0000 0000 RW: 1 DA: 04 MD:0

Time Cycle 8

R4: 0000 0010

Fields not specified above have fixed values throughout or are unused: SH. Based on the register contents, the branch is taken. The data hazards are avoided, but due to the control hazard, the last two instructions are erroneously executed.

11-18.*



11-22.*

(a) Add with carry

Action	Address	MZ	CA	RW	DX	MD	BS	PS	MW	FS	LC	MA	MB	AX	BX	CS
$R_{31} \leftarrow CC \wedge 00010$	AWC0	01	02	1	1F	0	00	0	0	8	0	10	1	00	00	11
$R_{16} \leftarrow R[SA] + R[SB]$	AWC1	01	00	1	10	0	00	0	0	2	0	00	0	00	00	00
if (R_{31}=0) $MC \leftarrow AWC5$ else $MC \leftarrow MC + 1$	AWC2	11	AWC5	0	00	0	00	0	0	0	0	00	0	1F	00	00
$MC \leftarrow MC + 1$ (NOP)	AWC3	01	00	0	00	0	00	0	0	0	0	00	0	00	00	00
$R[DR] \leftarrow R_{16} + 1$	AWC4	01	01	1	01	0	00	0	0	2	0	00	1	10	00	11
$MC \leftarrow IDLE$	AWC5	00	IDLE	0	00	0	00	0	0	0	0	00	0	00	00	00

(a) Subtract with borrow

Action	Address	MZ	CA	RW	DX	MD	BS	PS	MW	FS	LC	MA	MB	AX	BX	CS
$R_{31} \leftarrow CC \wedge 00010$	SWB0	01	02	1	1F	0	00	0	0	8	0	10	1	00	00	11
$R_{16} \leftarrow R[SA]–R[SB]$	SWB1	01	00	1	10	0	00	0	0	5	0	00	0	00	00	00
if (R_{31}≠0) $MC \leftarrow SWB5$ else $MC \leftarrow MC + 1$	SWB2	11	SWB5	0	00	0	00	1	0	0	0	00	0	1F	00	00
$MC \leftarrow MC + 1$ (NOP)	SWB3	01	00	0	00	0	00	0	0	0	0	00	0	00	00	00
$R[DR] \leftarrow R_{16} - 1$	SWB4	01	01	1	01	0	00	0	0	5	0	00	1	10	00	11
$MC \leftarrow IDLE$	SWB5	00	IDLE	0	00	0	00	0	0	0	0	00	0	00	00	00

11-24.*

Memory Scalar Add (Assume R[SB] > 0 to simplify coding)

Action	Address	MZ	CA	RW	DX	MD	BS	PS	MW	FS	LC	MA	MB	AX	BX	CS
$R_{16} \leftarrow R[SB]$	MSA0	01	00	1	10	0	00	0	0	0	0	00	0	00	00	00
$R_{18} \leftarrow R_0$	MSA1	01	00	1	12	0	00	0	0	0	0	00	0	00	00	00
$R_{16} \leftarrow R_{16} - 1$	MSA2	01	01	1	10	0	00	0	0	5	0	00	1	10	00	11
$MC \leftarrow MC + 1$ (NOP)	MSA3	01	00	0	00	0	00	0	0	0	0	00	0	00	00	00
$R_{17} \leftarrow R[SA] + R_{16}$	MSA4	01	00	1	11	0	00	0	0	2	0	00	0	00	10	00
$MC \leftarrow MC + 1$ (NOP)	MSA5	01	00	0	00	0	00	0	0	0	0	00	0	00	00	00
if ($R_{16} \neq 0$) $MC \leftarrow MSA2$ else $MC \leftarrow MC + 1$	MSA6	11	MSA2	0	00	0	00	0	0	0	0	00	0	10	00	00
$R_{18} \leftarrow M[R_{17}] + R_{18}$	MSA7	01	00	1	12	1	00	0	0	0	0	00	0	11	12	00
$R[DR] \leftarrow R_{17}$	MSA8	01	00	1	01	0	00	0	0	0	0	00	0	11	00	00
$MC \leftarrow IDLE$	MSA9	00	IDLE	0	00	0	00	0	0	0	0	00	0	00	00	00