Solutions to Problems Marked with a * in
Logic and Computer Design Fundamentals, 4th Edition

Chapter 12

12-1.*

Heads x (cylinders/Head) x (sectors/cylinder) x (1 cylinder/track) x (bytes/sector)

a) 1 x 1023 x 63 x 512 = 32,224.5 Kbytes (K = 1024)

b) 4 x 8191 x 63 x 512 = 1,032,066 Kbytes

c) 16 x 16383 x 63 x 512 = 8,257,032 Kbytes

12-5.*

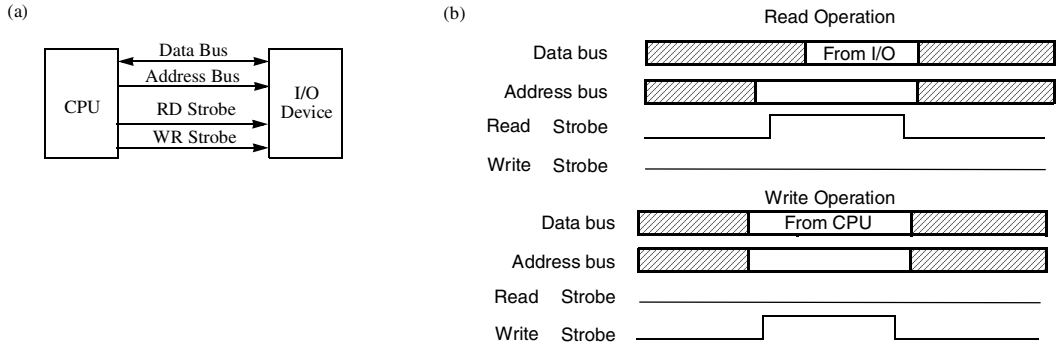
a) If each address line is used for a different CS input, there will be no way to address the four registers so 2 bits are needed to address the registers. Only 14 lines can be used for CS inputs permitting at most 14 I/O Interface Units to be supported.

b) Since two bits must be used to address the four registers, there are 14 bits remaining and 2^{14} or 16,384 distinct I/O Interface Units can be supported.

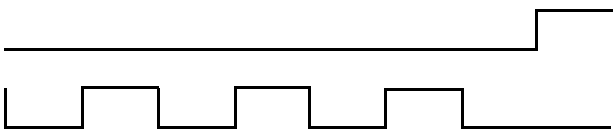
12-7.*

A given address can be shared by two registers if one is write only and one is read only. If a register is both written to and read from the bus, then it needs its own address. An 8-bit address provides 256 addresses. Suppose that the 50 % of registers requiring 1 address is X. Then the remaining 50 % of the registers, also X can share addresses requiring only 0.5 addresses. So 1.5 X = 256 and X = 170.67 registers for a total of 341.33 registers. To meet the original constraints exactly, the total number of registers must be divisible by 4, so 340 registers can be used, 170 of which are read/write, 85 of which are read only and 85 of which are write only. There is one more address available for either one read/write register or up to a pair with a read only register and a write only register.

12-9.*



12-11.*



There are 7 edges in the NRZI waveform for the SYNC pattern that can be used for synchronization.

12-13.*

SYNC 8 bits	Type 4 bits 1001	Check 4 bits 0110	Device Address 0100111	Endpoint Address 0010	CRC	EOP

(a) Output packet

SYNC 8 bits	Type 4 bits 1100	Check 4 bits 0011	Data 01000010100111101010011 0	CRC	EOP

(b) Data packet (Data0 type) (bits LSB first)

SYNC 8 bits	Type 4 bits 0111	Check 4 bits 1000	EOP

(c) Handshake packet (Stall type)

12-16.*

Description	Device 0				Device 1				Device 2			
	PI	PO	RF	VAD	PI	PO	RF	VAD	PI	PO	RF	VAD
Initially	0	0	0	-	0	0	0	-	0	0	1	-
Before CPU acknowledges Device 2	0	0	1	-	0	0	0	-	0	0	1	-
After CPU sends acknowledge	1	0	1	0	0	0	0	-	0	0	1	-

12-18.*

Replace the six leading 0's with 000110.

12-20.*

This is Figure 13-17 with the Interrupt and Mask Registers increased to 6 bits each, and the 4x2 Priority Encoder replaced by a 8x3 Priority Encoder. Additionally, VAD must accept a 3rd bit from the Priority Encoder.

12-22.*

When the CPU communicates with the DMA, the read and write lines are used as DMA inputs. When the DMA communicates with the Memory, these lines are used as outputs from the DMA.