
THE UNIVERSITY OF QUEENSLAND

# Embedded Hardware for a Humanoid

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**Submitted for the degree of**
**Bachelor of Engineering (Electrical and Electronic), Minor in Mechatronics**

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# Statement of Originality

Simon Matthews-Frederick

28 October 2003

The Head
School of Information Technology and Electrical Engineering
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Dear Professor Kaplan

In conforming to the requirements of the completion of a Bachelor of Engineering in the division of Electrical Engineering, I present the following thesis:

**'Embedded Hardware for a Humanoid'**

This thesis was produced under the supervision of Dr. Gordon Wyeth.

I declare that the work contained within has not been previously submitted at any tertiary institution. This thesis contains no material published by any other person, except where a reference is made.

Yours Sincerely

Simon Matthews-Frederick

# Abstract

Now in its third year of development, the GUROO project, a platform for the investigation into humanoid robotics was brought to working order last year. The first generation of hardware worked well enough for GUROO to take his first steps and enable significant work to be undertaken in gait generation and development of a walking algorithm. However as with all first generation products, after time, the system has been found inadequate for future development and a new system must be designed to enable the system to continue to progress. This thesis "Embedded Hardware for a Humanoid" has been involved in analyzing the current system along with a design proposed last year and has come up with a new hardware design that will be faster, more efficient and ready for the future of the GUROO project. The main areas of improvement have been:

- Upgrading the CPU, which will enable faster cycling of the control loop resulting in more accurate motor control and more motors to be controlled per board.
- Moving to a more efficient design by using two cascaded SMPS to regulate the power supply from one set of batteries.
- Changing the motor driver to a semi-discrete H-bridge design to further increase efficiency.

The improvements have been integrated together to produce a new design ready for construction in the near future. The hardware design proposed by this thesis will provide a platform for further software development that will result in GUROO, someday playing soccer.

# Acknowledgements

The following people have been invaluable in their help in completing this thesis; I wish to thank them for their assistance:

Gordon Wyeth, for his supervision and open ear for all things technical.

Damien Kee, for always lending a helping hand and not hesitating to spend time explaining the finer points of GUROO.

Douglas Turk, for helping with the GUROO-ROBOROO's processor homogenization, especially with memory selection.

Geoff Walker, for explaining the finer points of motor drive and power electronic operation.

My housemates and friends, for their understanding of my work and encouraging me to often get out and forget it.

My family, for their ongoing support and help in whatever pursuit I find myself undertaking.

The 2003 GUROO team, for their understanding of the pain that goes into completing such a project.

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# 1. Introduction

" Design and implementation of embedded hardware for a humanoid"

The above statement gives a broad description of the thesis completed in 2003. The humanoid in question is GUROO, a humanoid designed at the University of Queensland in 2001. In 2002 GUROO was built and took his first steps. Also in 2002 GUROO competed at the RoboCup competition in the inaugural humanoid league competition. In 2003 this thesis deals with the implementation and design of new distributed motor controllers, primarily designed for control of the high power DC motors in the lower body. Some work has already been completed in this area with A. Hood completing a thesis in 2002 titled "Distributed motion controllers for a humanoid". This thesis somewhat follows on from this work and proposes a complete redesign of the current system.

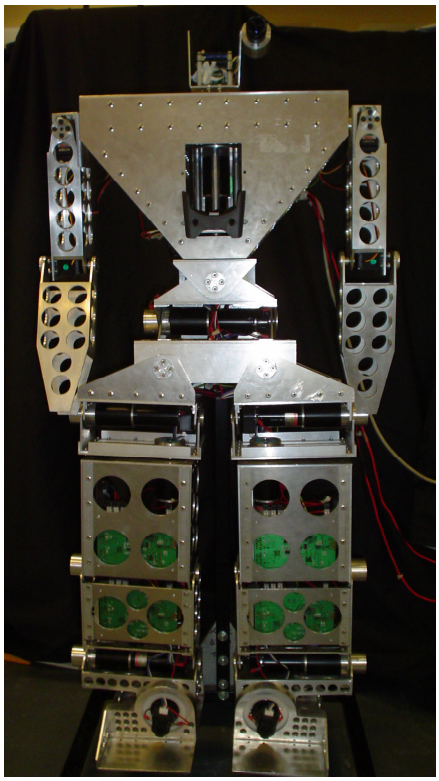


*Figure 1: GUROO (28/10/03)*

## 1.1 Thesis Overview

After three years of development GUROO is at a stage where major software development can take place. The first two years were spent designing and building the platform for this development. The mechanical design and construction used has been found appropriate, the distributed control system however, has not met the initial aspirations of the project. Therefore in an attempt to bring the electronics back into line with the rest of the system this thesis has been completed. The main areas of improvement have been:

- Allowing the PID control algorithm to loop faster, at least to the original specification of 2kHz
- Reducing the complexity of the wiring harness on GUROO
- Increasing efficiency in both the power regulation and motor drive electronics
- Allowing the hardware to accept external sensors that may be added in the future
- Expanding the memory available for the controllers to allow them the capability to become more intelligent

After the selection of main components was completed a detailed schematic of the boards was constructed with all peripheral components included. This schematic was the main deliverable of this thesis. It is expected that in the near future the PCB layout and routing will be completed and the boards integrated into GUROO.

## 1.2 Thesis Goals

The main goal of this thesis was to produce a hardware design that addresses all of the shortcomings in the original boards. It was also specified that the new design was to use the same processor as the ROBOROOS team. By doing so, the processors used in the robotics lab would become standard and allow the sharing of development tools as well as expertise. This homogenization would benefit both teams, as they will be able to work together a lot more than is possible at the current time.

## 1.3 Chapter Outline

1. Introduction

An overview of the thesis including goals and a summary of other GUROO team members

2. Review of Past Designs

A review of past designs related to GUROO and motor control including Kennedy's work in 1999 on the distributed control of a PUMA arm, Stirzaker and Cartwright's 2001 hardware design currently used on GUROO, and Hood's 2002 design of an improved distributed control

system. The shortfalls and strong points of each design are analyzed to give an idea of where this thesis is heading.

3. New Design Specifications

The argument for a new design is put forth along with the performance specifications for each section of the design.

4. Design Components Selection and Calculations

This section details the decisions made in selecting the components along with the calculations required for making such decisions. Other components that were considered for use are also discussed.

5. Testing and Results

The test procedures carried out on the new power electronics design is discussed in this section. A comparison of the new design's experimental performance against the calculated and previous designs results is also included in this section.

6. Board Layout and Placement

Where to place the controller boards into GUROO, as well as the layout of components on each board is outlined in this chapter.

7. Future Work

This section details the work still needed to bring the new design into working order. Also included is where the project could go in the future.

## 1.4 Team Members

Many other team members have been involved with the design and construction of GUROO over the last three years; their work can be viewed in the following undergraduate theses.

| Author | Title | Year |
|---|---|---|
| Toby Low | Active Balance System for a Humanoid Robot | 2003 |
| Tim Pike | Gait Generation for a Humanoid Robot | 2003 |
| Anthony Peters | Vision Software for Humanoid Robot Soccer | 2003 |
| Nick Undery | Walking Software for a Humanoid | 2004 |
| Andrew Hood | Distributed Motion Controllers for a Humanoid Robot | 2002 |
| Adam Drury | Gait Generation and Control Algorithms for a Humanoid | 2002 |
| Ian Marshall | Active Balance Control for a Humanoid | 2002 |
| Jarad Stirzaker | Design of DC Motor Controllers for a Humanoid | 2001 |
| Tim Cartwright | Design and Implementation of Small Scale Joint Controllers for a Humanoid | 2001 |
| Damien Kee | Design and Simulation of a Humanoid Drive System | 2001 |
| Mark Wagstaff | Mechanical Design and Internal Sensors for a Humanoid | |

*Table 1: GUROO Team Members*

# 2. Review of Past Designs

The relatively new field of humanoid robotics includes two main groups of developers. Those developed for commercialization and those developed for research. Two companies involved with humanoid robotics, Sony and Honda both have working models. ASIMO is 10th in a line of humanoids built by HONDA in the last 17 years. She is 120cm tall, with speech synthesis, ambidextrous hands and stereo vision [1]. The robot walks smoothly and can climb stairs.
Sony's SDR-4X is 50cm tall, weighs 6.5kg and uses a pair of 64-bit processors, it also incorporates stereovision, speech recognition and speech synthesis to a purchasable product [2].

*Figure 2 - Honda's ASIMO*

GUROO, developed at the University of Queensland is currently in its third year of development. Achievements last year include the mechanical construction and incorporation of the joint controllers to allow GUROO to take his first steps. This year it is hoped to integrate the vision system into the robot as well as an inertial sensor, these sensors will allow GUROO to become more aware of his environment and some level of global feedback will be given to the motor controllers. This thesis will contribute to the project by supplying motor controllers able to operate at speeds in excess of the final goals of the project, if completed successfully these should be the final controller boards required to enable GUROO to reach his final goal of playing soccer.

## 2.1 Review of Current Design (2001, Stirzaker & Cartwright)

The motor controller boards located in GUROO at this point in time are those designed by Stirzaker [3] and Cartwright [4] in 2001. Their designs were based upon work done on a PUMA robotic arm by Kennedy in 1999 [5]. Kennedy's design was different from normal control of an arm as it ran all its central processing and power hardware in a box and ran motor power cables to each joint individually. Each motor had its own local controller board in the box which was controlled by a central processor, this central CPU broadcast the movement that was required by the joints onto a data bus and the local controller boards selected which

information they required for movement. This system greatly simplifies wiring complexity and allows the control and intelligence to be split into modular components, so they can be upgraded separately. This system was ideal for a humanoid robot as most of the free space is close to the motors, in the legs and arms and not in a central location such as the head or chest. In the GUROO design it was decided to use 5 controller boards, which would each control 3 of the high power DC motors in the lower body. Another single board was used to control the low power servomotors in the head and arms. The servo motor control board is practically identical to the rest of the boards with all the motor drive circuitry replaced by a logic tri-state buffer. The communication standard used between the central control system and the distributed motor controllers is CAN (Controlled Area Network) [6]. Bosch developed the system for the automotive industry; it is a multi-master system with software identifiable nodes [6]. A 2-wire bus is all that is required for the physical system. The CAN standard contains sophisticated error checking and is capable of data rates greater than 1Mbps. The controller boards use a 16-bit DSP from Texas Instruments as their processor to run the control loop. Also on the boards are various peripherals, some which are necessary are current and motor position sensing, motor drive circuitry and some interfacing chips to the CAN and SCI buses. The board is powered from two rails 42V for the motors and a 7.2V supply that is regulated to 5V to power all the digital circuitry.

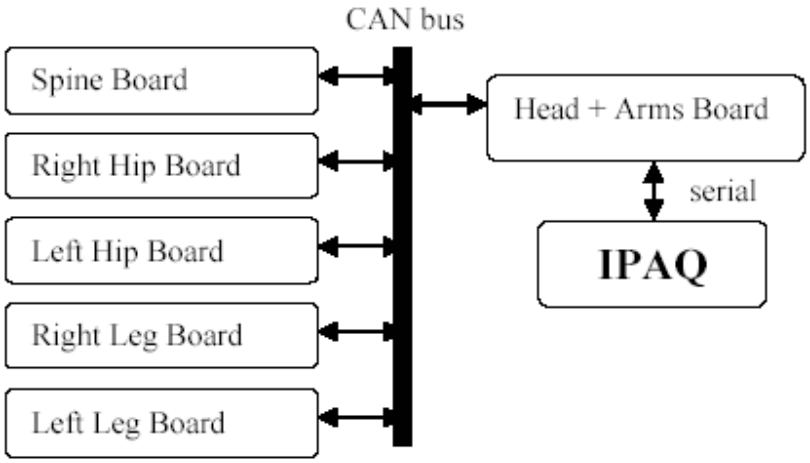



*Figure 3: Current Distributed Control System [8]*

### 2.1.1 Microcontroller Selection

Currently used in GUROO is the TMS320F243, this processor is used to cycle a PI (proportional + integral) control loop to maintain 'good' control of the motor. Kennedy's PUMA arm controller [5] used a 16-bit DSP with built in quadrature decoding and PWM generation and ran the control algorithm at 20kHz, this allowed the joints to move at very high speeds, as GUROO's joints will never move that fast, a cycling frequency of 2kHz was decided upon if running a similar DSP. Other necessary functions were:

- Analogue to Digital converter
- In-circuit programming
- CAN interfacing

Of the 16 and 32 bit processors that have the required options the only two ideal chips were the Motorola 68376 and the TI TMS320F243. The TI chip was chosen due to availability and cost. Other features of the TI chip include:

- 20 MIPS
- An event manager which has
    - 2x general purpose timers
    - 3x capture units, 2 with quadrature decoding
    - 3x 16 bit full compare units
- CAN module
- SCI module
- 8 channel ADC

The Motorola 68376 is however, a superior chip as it can control more motors and loop at speeds in excess of the specifications. In retrospect it seems that the wrong decision was made, as the main problem with the current boards is the loop speed. A benefit in using the TMS is that it has in-built FLASH and SRAM allowing the board size to be reduced and the external bus is used to interface external quadrature decoders. If the 68376 were used, its bus would be used for interfacing external memory, this would not be a disadvantage as it has a 16-channel

TPU that can be used for quadrature decoding, and the TPU would allow for much faster control of more motors.

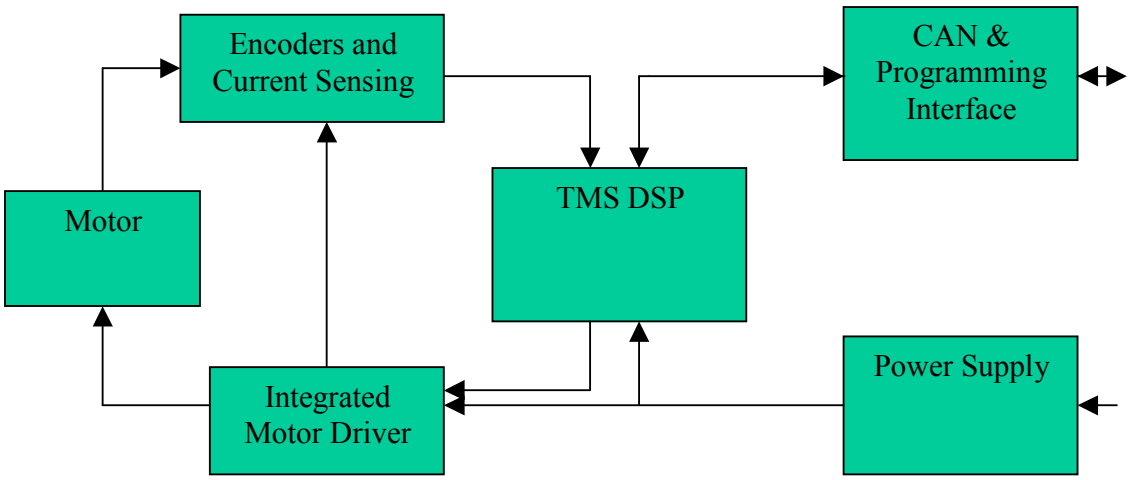



*Figure 4. Block Diagram of Current Controller Boards*

### 2.1.2 H-Bridge

To gain control of a motor in all 4 quadrants of the current-voltage plane then a full-bridge switch-mode class D amplifier is the only way to do it. A H-bridge configuration consists of two legs of two switches in series, from power to ground, with the motor branching from in between. Diodes are placed in anti-parallel with the switches to allow current to flow constantly in the motor. The best devices for switching this type of circuit is the MOSFET used in saturation as they can switch at high frequencies and can handle high power. Shown below are the four practical states for the bridge to be in.

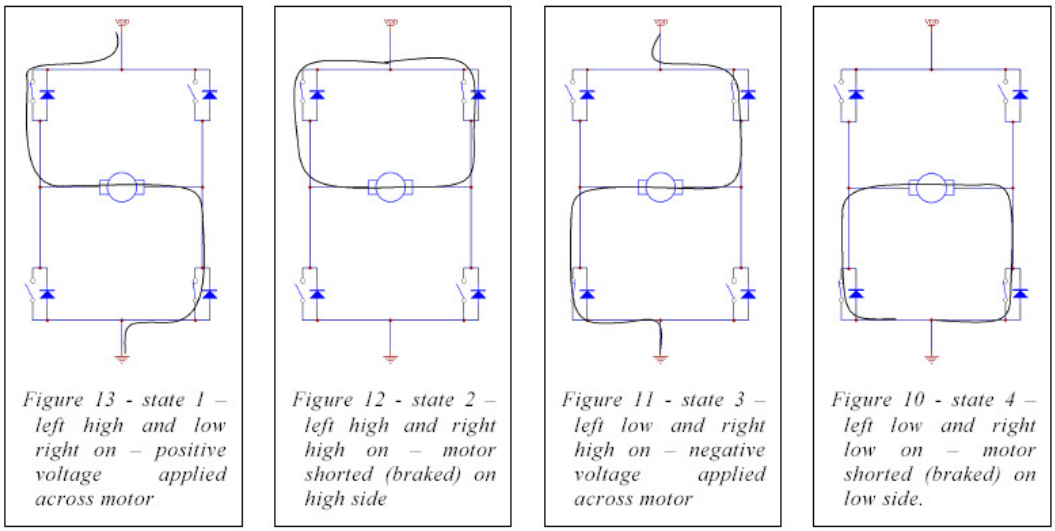


*Figure 13 - state 1 – left high and low right on – positive voltage applied across motor*

*Figure 12 - state 2 – left high and right high on – motor shorted (braked) on high side*

*Figure 11 - state 3 – left low and right high on – negative voltage applied across motor*

*Figure 10 - state 4 – left low and right low on – motor shorted (braked) on low side.*

*Fig 5: States of a H-Bridge [7]*

The most common ways of controlling the h-bridge is to use either uni-polar or bi-polar switching. Bi-polar switching is the easiest to implement and uses stage 1 for the positive cycle and stage 3 for the negative cycle. Stages 2 and 4 are not used in this method. To keep the motor still the duty cycle is kept to 50% and therefore achieves an effective zero volts across the motor. To drive the motor forward the positive time is increased, and vice-versa.

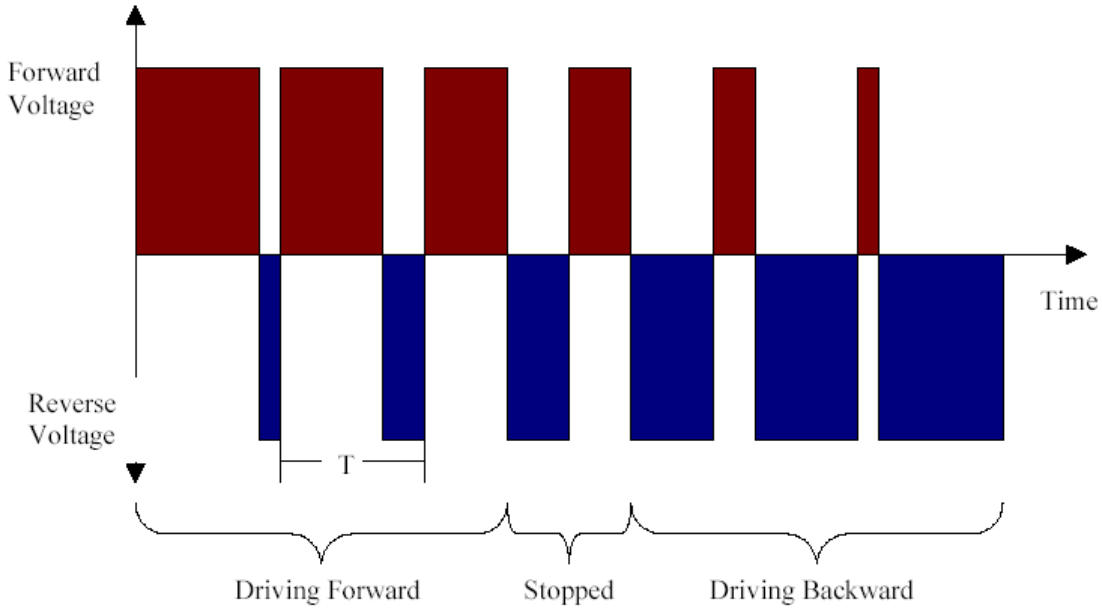



*Fig 6: Bi-polar switching [5]*

In Uni-polar switching all four states are used. On one leg of the h-bridge one switch is kept open, the other side then switches between its high and low side with a duty cycle proportional to the power delivered. When the direction of the motor is to be changed the side that was switching holds one transistor open and the other side starts switching. This is not true uni-polar switching but a slightly less efficient method sometimes called one-phase chopping.

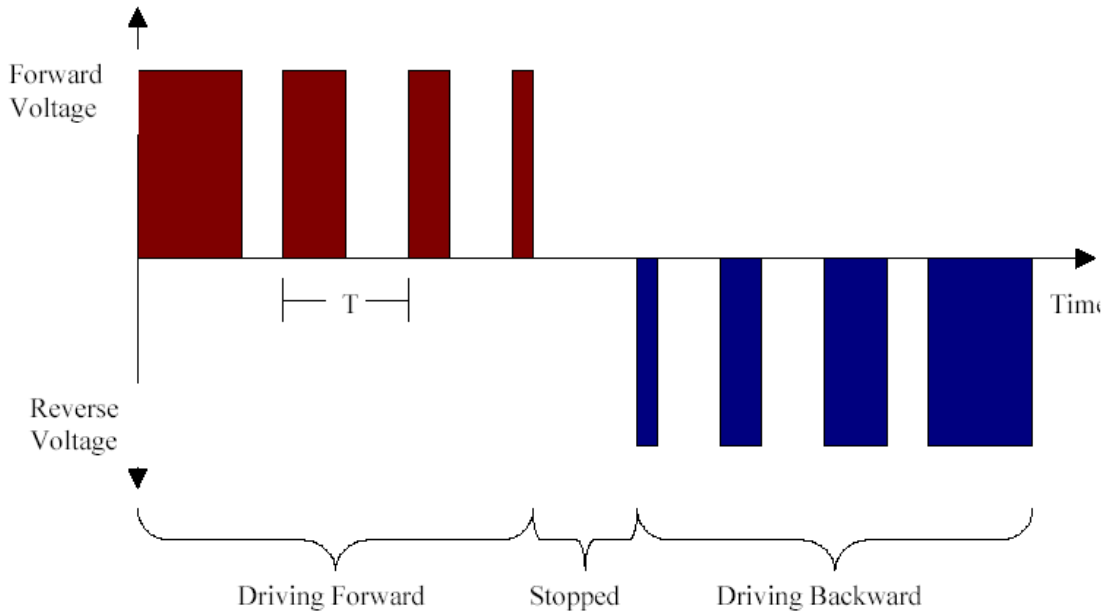



*Fig 7: Uni-polar switching (one-phase chopping) [5]*

Stirzaker chose to implement the h-bridge as a fully integrated package, the ST16203. The integrated option was chosen as it was thought there was going to be a lack of space for the boards and the integrated solution was the most compact. The chips are mounted down one edge of the board and are wearing large heatsinks to dissipate the wasted energy caused by the bi-polar switching used. Due to the design of the integrated solution bi-polar switching is forced. When the motors were driven it was seen that they were dissipating more heat than was safe for them to do so. To reduce the motor heat the ripple current was minimized by adding extra inductors, allowing the motors to experience much smoother current and to run cold.

### 2.1.3 Current Sensing and Motor Protection

The two cases that could cause damage to the motors:

- Motors are being overdriven
- Driver circuit failure

The first case is compensated for in software on the first generation boards, the current sensing circuitry reports back to the CPU and when the power approaches a dangerous level the PWM is limited to lower the current through the motor. If the software fails to limit the PWM to a safe level or the driver circuit fails a hardware mechanism is in place that will trigger the !PDPINT of the CPU. When this pin is driven low the PWM will be shut off within 12ns. The current sensing circuitry consists of a low ohmic resistor between the lower MOSFETS and ground and an amplifier. The small voltage across the resistor is amplified and fed into the ADC of the CPU and software can then be utilized to solve for the current. For the hardware protection method, the amplified voltage is compared against a voltage tuned by a potentiometer and if the result indicates excess current the !PDPINT is triggered. If the MOSFET's fail and the power to the motor is shorted to ground a fuse is in place to stop damage if both previous methods fail.

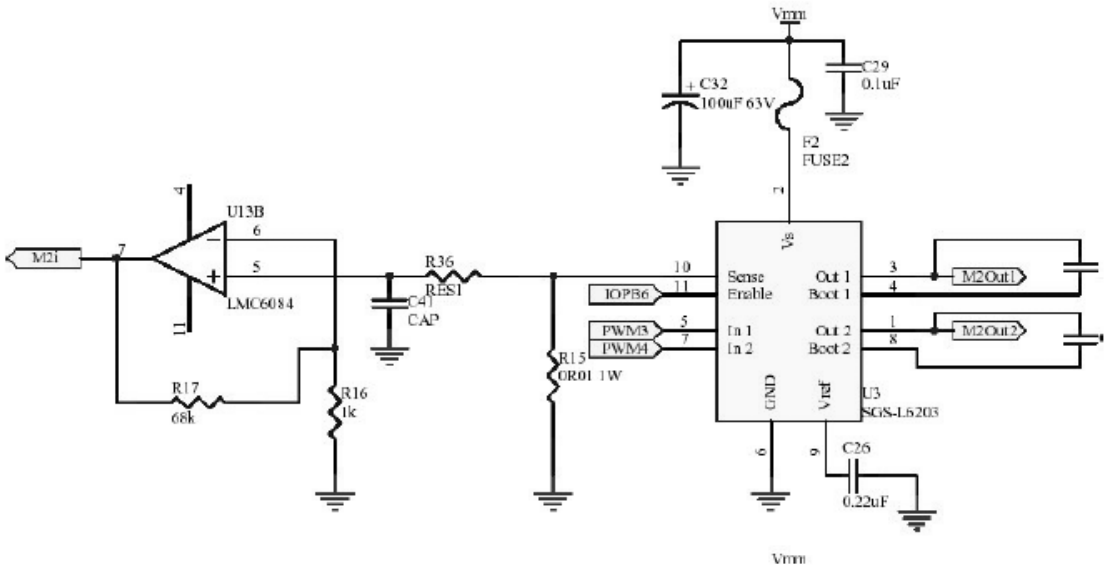



*Fig 8: current sensing circuit [7]*

### 2.1.4 Power Supply

The current power system designed for GUROO uses two supply rails, one 42V supply for the motors and another 7.2V rail to run the digital circuitry. Both rails are supplied directly from packs of batteries, the red 42V NiMH cells are connected in parallel to supply the motors and are housed in the torso where there is space to hold 4 of these packs. 2 green RC batteries supply the 7.2V rail; one supplies power for the eight servomotors and the other is for all digital circuitry on all boards. All the batteries go through a PCB, which distributes power to all the boards, the PCB contains diodes to let current only flow out of the batteries and fuses to protect the batteries from components drawing too much current. The DC motor boards currently draw about 300mA at 5V and the motors draw a typical value of 1A when under load [7].

### 2.1.5 Selection of Peripherals

**CAN:**

Only 2 CAN transceivers were found that operate on 5V those being the Philips PCA82C250 and the TI SN65HVD230. The TI chip was disregarded as it was only available direct from TI and had no great advantage over the Philips chip. The only feature on this chip that really makes any difference is the high-speed mode. This feature may allow the CAN bus to transmit data at up to 2Mbit/s, at the moment this feature isn't really usable as the bottleneck in speed for the bus is at the central computer and an increase in bus speed will make no difference to the speed at which signals reach the distributed controllers.

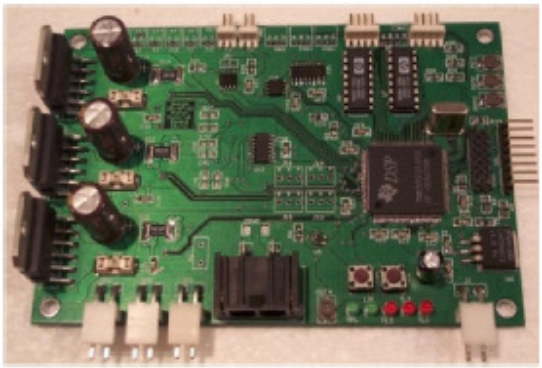


*Figure 9: 2001 Controller Board*

**SCI:**

More options were available when looking for an SCI transceiver. The MAX323 was chosen for its low price, small size and availability. The MAX contains one transmitter and receiver, which is all that is required for this application.

**Reset chip:**

The reset chip is required to hold the reset line of the CPU low for a period of time to make sure the CPU is reset properly when the reset pushbutton is pressed. The MAX811 has been used for the previous joint controllers and there was no reason to change away from the cheap MAX811 for the current design.

## 2.2 Review of 2002 Proposed Design (Hood, 2002)

After the first hardware design was completed, ways to improve on the performance were started on immediately. Andrew Hood partly completed a hardware design in the second part of his thesis "Distributed Motion Controller for a Humanoid"; in the following section the design proposed there is discussed.

The design outlined by Hood is based upon the current system in place. Using a CAN bus for communication and a TMS series processor. The aims of the design were similar to this thesis being:

- The control loop cycle speed must be increased
- A mechanism to align the joints must be put in place
- The motor power supply must be made more efficient

A detailed discussion of the choices made by Hood can be viewed in his thesis; the following section will only give a brief overview of the ideas proposed.

### 2.2.1 Microcontroller

A TI TMS320F243 was chosen as the CPU, this is the next generation of TMS controller from the chips used in the current design. Running at 40MHz the control algorithm would run well in excess of the specification of 2kHz, therefore meeting aim one. Using this controller, two motors are driven per board and the quadrature decoding is done internally. This is the main problem with Hood's design. With only two motors controlled per board the number of boards would have increased to eight and would cause a complication in wiring and fill the body of GUROO with electronics. With the addition of an inertial sensor and vision, the space within

GUROO is quickly filling up, and does not need extra motor controller boards taking up valuable space.

### 2.2.2 H-Bridge

When looking to increase the efficiency of the motor drive circuitry a semi-discrete H-Bridge solution was decided upon. Using IRFZ44VS MOSFET's and a HIP4081 driver, the design has merit. The HIP is an easy to use chip, has protection from shoot-through and has a relatively small number of external components. The IRFZ44 in a D2 pack has a very small on resistance and high power dissipation, which makes them ideal for a H-Bridge situation. This design adds many more components to the current design with four FET's and a driver per motor. The extra space required is insignificant to the amount of power saved.

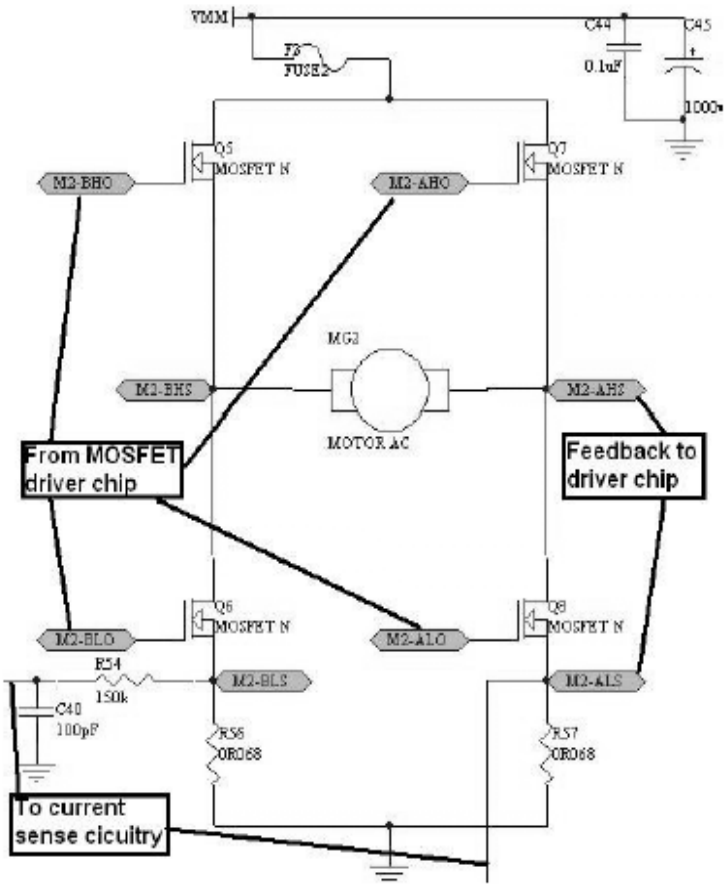



*Figure 10: Semi-Discrete H-Bridge [7]*

### 2.2.3 Current Sensing and Motor Protection

As one-phase chopping was proposed as a switching method, the most common way to sense current in a H-Bridge is to place low-ohmic sense resistors in series with the lower legs of the bridge. The voltage across these resistors is amplified and fed into the ADC of the CPU for processing. The design is the same as the system used in the current system, as it works well and protects against all foreseen problems.

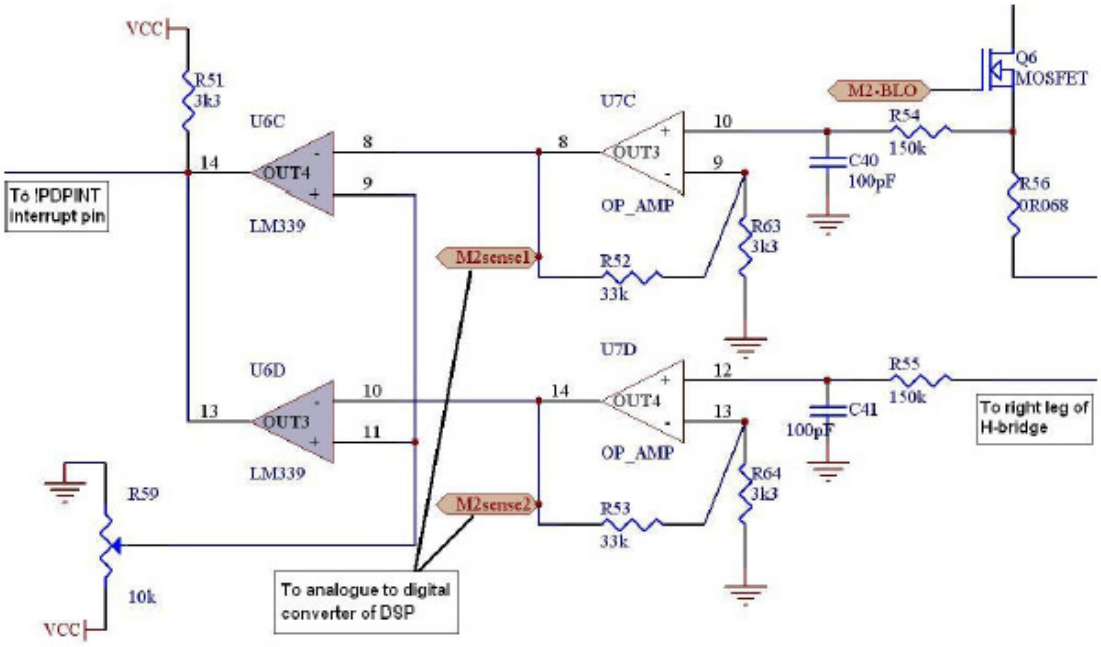



*Figure 11: Current Sensing Circuitry in 2002 Design [7]*

### 2.2.4 Power Supply

Hood made a major improvement to the current system in terms of the power supply. A switch-mode chip, the LT1676 was chosen and two examples were used per board. The 48V supply was regulated to the two levels required for the board, 12V and 3.3V. This idea of regulating the 48V reduces the wiring between boards and eliminates the need for the 7.2V battery. The switch-mode design further increases power efficiency and the LT1676s are simple to integrate into the system making for a much-improved design.

### 2.2.5 Peripherals

Three peripheral chips are required for the controllers to slot into the existing system.

1. CAN transceiver
2. SCI chip
3. Reset chip

The selection of these were made simple by the lack of choice, as the parts had to powered from the 3.3V supply, there are no real improvements to the system by the selection of the following chips:

1. TI SN65HVD230 CAN transceiver
2. MAX3221 SCI
3. MAX811 reset chip

# 3. New Design Specifications

At the conclusion of 2002 Hood's design may have seemed perfect and expected to be built and integrated in 2003. By the time this thesis had started, however, the design specifications had changed. Namely homogenizing the CPU's used by the two robotics teams (GUROO and the ROBOROO's) in room 311. When a CPU was selected that met both the team's needs it was no surprise that the device chosen was not the one proposed in 2002. With a new processor to use, a complete new design had to be drawn. After looking at all the previous designs completed, and taking into account the new recommendations, a new design has been proposed based on the following specifications.

### 3.1 Microcontroller

As discussed above, the main stipulation when selecting a microcontroller was the need to use the same processor as the ROBOROO's team. Also a main requirement was the ability to perform quadrature decoding internally. On the current system the quadrature decoding is completed externally and results broadcast onto the data bus of the TMS, the speed at which the decoding is completed is the only part of the control loop that runs below spec and drags the whole system down with it. A 32-bit processor running at 20MHz at least was needed to perform the calculations. As the ROBOROO's team currently uses a Motorola 68K series processor and has all the programming software understood, this family was looked into closely. Other necessary functions were:

- Analogue to Digital converter
- In-circuit programming
- CAN interfacing

Depending on the processor selected interfacing to external Flash and SRAM may be necessary if the required level of memory is not integrated into the microcontroller.

### 3.2 H-Bridge

In terms of the H-Bridge, the decision was made to move to uni-polar switching to improve efficiency and reliability. Another specification was to change the topology of the circuit from a totally integrated package to a semi-discrete solution comprising of a driver chip and four power MOSFET's in the H-Bridge arrangement. The main goal here was to reduce power dissipation in the circuit to a level where little or ideally, no heatsinking would be required. As the topology of the circuit was specified, the components need to be selected to complete the design.

### 3.4 Current Sensing and Motor Protection

Looking back at all the previous designs the current sensing and motor protection circuitry has kept a similar topology every time. As the motor protection is seen to be adequate, the design will only need to be modified slightly to allow integration into the semi-discrete design of the H-Bridge. The main functionality can be seen in the block diagram below, the sense resistors are placed in series with the lower legs of the H-Bridge. The voltage across the sense resistor is amplified and fed into the A/D of the CPU. The processor can then calculate the current flowing through the legs of the H-Bridge.

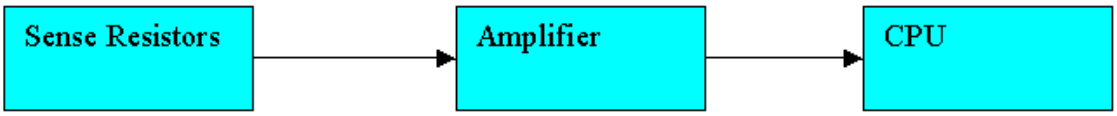



*Figure 12: Block Diagram of Current Sensing Circuitry*

### 3.5 Power Supply

The main requirement for a new power supply design is to power the boards off one supply rail, as opposed to the two that are currently required. Also needed is a more power efficient design. By powering the boards off one rail the benefits include:

1. Reducing the complication of the wiring on GUROO to a single set of power cables to each board.
2. By eliminating the 0.5kg of batteries that are needed for powering the digital circuitry. Reducing the weight would increase efficiency as well as lessening the load on the motors; this lessened load may lead to increased accuracy and speed within the joints.

Looking at previous designs, the only option is to move to a switch mode power supply regulated to the various levels that are required. An integrated package for the converter should be used to minimize the external components required and the complexity of construction.

### 3.6 Peripherals

The three peripheral chips present in the current design will again be required:

1. CAN transceiver
2. SCI interface
3. Reset chip for the CPU

Selection of these devices will depend on the voltage levels available, as there are 3.3V and 5V variants on the market. Most of the chips perform exactly the same job and have the same footprint, therefore selection will be based upon availability and cost.

### 3.7 Connections

Standard IDC locking headers have been specified for data connections, the same connectors that are used in the current system. As far as motor and power connectors, the power headers can once again be used, though there has been a suggestion to change to the connectors used by Kennedy on the PUMA control boards. The power headers must be small, able to handle the currents present and be daisy chained to reduce wiring.

# 4. New Design Component Selection and Calculations

The majority of this thesis has been involved with the selection of components to use in the new hardware design. Chapter four details this selection process, both of the components and circuit topologies. Following the specifications outlined in the previous section a new design was completed that meets all required goals and hopefully will stay with GUROO for some time.

## 4.1 Microcontroller Selection

As the whole design is based around the CPU, the first step in the new design process was to select a microcontroller. Three processors were found which fulfilled the design specifications and were available for use:

1. Texas Instruments TMS320LF2406
2. Motorola MPC555
3. Motorola MC68376

After consultation with the ROBOROO's team the TI device was eliminated as it did not provide for enough motor control with only two internal quad decoders. The Motorola chips are similar in construction, both featuring Motorola's TPU (Time Processor Unit), which was the main draw card to these products. The TPU is said to be an intelligent, semi-autonomous microcontroller designed for timing control. Operating simultaneously with the CPU32, the TPU schedules tasks, processes microcode ROM instructions, accesses shared data with the CPU32, and performs input and output functions. [9]

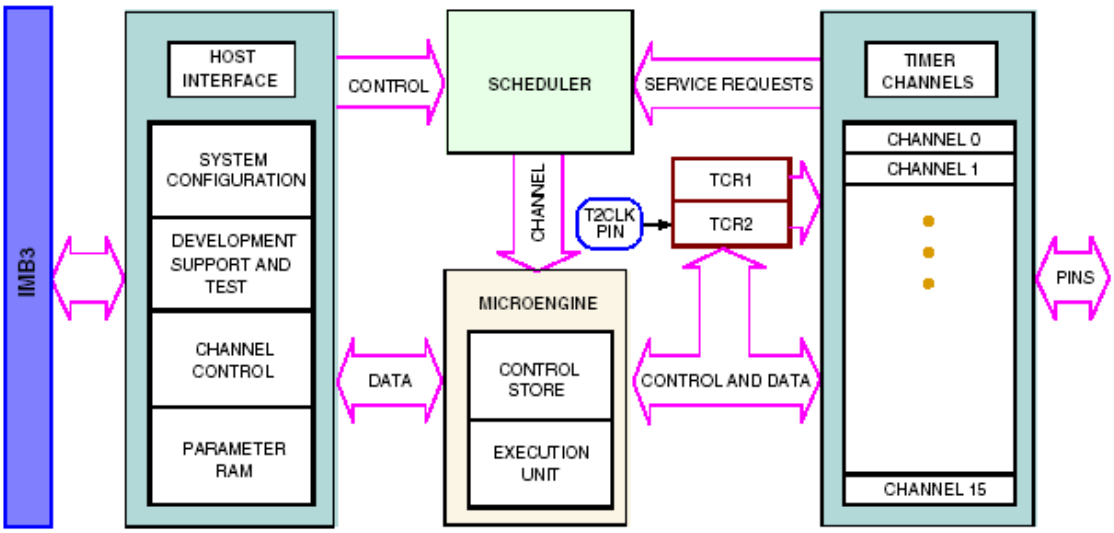



*Figure 13: Block Diagram of Motorola's TPU* [9]

Most importantly for the GUROO project the 16 TPU channels can be programmed to perform quadrature decoding, therefore allowing many more encoders to be connected than the TI device. The MPC555 was the initial favorite due to its dual TPU's and higher frequency of operation. The 555 is a chip designed for automotive use and only comes in a ball-grid array package, as the PBGA package requires special mounting equipment and hinders troubleshooting due to all the electrical connections being impossible to access, the package is where the 555 begins to fall down. Added to the package problems, the 555 has an internal FLASH write limit of 100 cycles, meaning after 100 times writing to the internal memory the program can never be changed again, as GUROO is a research tool the program running on the controller boards may well be changed every day and a limit of 100 write cycles is simply not feasible. The MC68376 was selected as the processor to use for the final design, with only one TPU and a slower operating frequency than the 555, it succeeds based on usability. The flat-pack package and use of the background-debugging mode for programming external memory make the 68376 a much more user-friendly product. Also to the 68376's advantages is the fact that the ROBOROO's team has been using 68K processors for some time and they have the development software already running. Other features of the Motorola MC68376 include:

- 32-bit Central Processing Unit (CPU32)
- System Integration Module (SIM) with external bus support
- Standby RAM Module (SRAM) 4Kb
- 16 channel, 10-Bit Queued Analog-to-Digital Converter (QADC)
- Queued Serial Module (QSM) supports both SCI and SPI
- Configurable Timer Module Version 4 (CTM4) including four pulse-width submodules
- Time Processor Unit (TPU)
- CAN 2.0B Controller Module (TouCAN)
- Intermodule Bus

After much calculation and rearranging of pin function it was decided the processor could support a maximum of five motors per board. This number is a major improvement over the 2002 design, which proposed two motors controlled per board. This design requires three boards for the 15 lower body motors and one board for the servomotors in the upper body, the positioning and arrangement of the boards will be discussed in the relevant section.

### 4.2 Memory Selection

The Motorola MC68376 selected for use in the new design does not have the inbuilt memory of the TMS DSP's used in the previous designs. As the 68376 only includes 4K of SRAM and no internal FLASH, extra memory is required in the new design to run the control loop and to allow the boards to be ready for the future, where the controllers may be expected to complete more functions than just motor control. The only real solution to the lack of memory is to use external SRAM and FLASH. The external chips were connected to the data bus of the CPU and controlled via the chip select lines of the processor. The selection of the devices was completed with involvement from the ROBOROO's team. In a bid to keep the processor circuitry relatively standard across the two teams, it was decided to use the same memory organization. The ROBOROO's have much larger programs running on their motor boards and therefore require more memory than the GUROO boards. For that reason the memory selection has been mostly based on the specifications set by the ROBOROO's, with the exception of the

requirement for a 16-bit wide address bus for the FLASH to allow the control loop to run effectively on GUROO.

### 4.3 FLASH selection

As far as the required specifications required for the FLASH, the most important was the 16-bit wide data bus. It was not possible to find a device that had a small package as well as a wide enough data bus. It was decided to use two 8-bit chips (see Logic Diagram below for connection requirements) and connect them onto the same address locations to make a 16-bit system. The ST M29F010B was chosen for the following features:

- Single 5v supply for program, read and erase functions
- 45ns access time
- 128kB of space per device
- Standby and automatic standby to reduce power consumption
- Small TSOP32 package

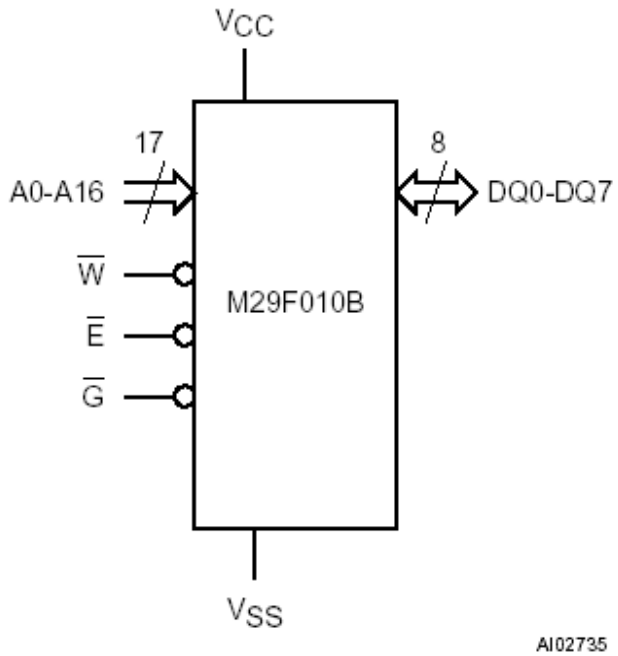



*Figure 14: FLASH Logic Diagram [13]*

### 4.4 SRAM selection

The MC68376 has 4k of internal SRAM, but this value is not large enough to allow the ROBOROO's team to run their on-board processing. 4k would give GUROO enough SRAM to

complete the control functions of the boards at the present time, if however the boards are required to perform more processing in the future, this small amount of SRAM would limit the boards capabilities. The SRAM chosen is an Alliance Semiconductor product, the AS7C31026, for its very low power consumption (880mW when active [14]) and fast access time (20ns max [14]). Other features include:

- Centre power and ground pins for low noise
- Small TSOP44 package

### 4.5 H-bridge

After the CPU was chosen the next part of the design completed was the H-Bridge. As outlined in the design specifications section, a semi-discrete solution for the motor driver was selected. In designing this part the topology is more or less set.

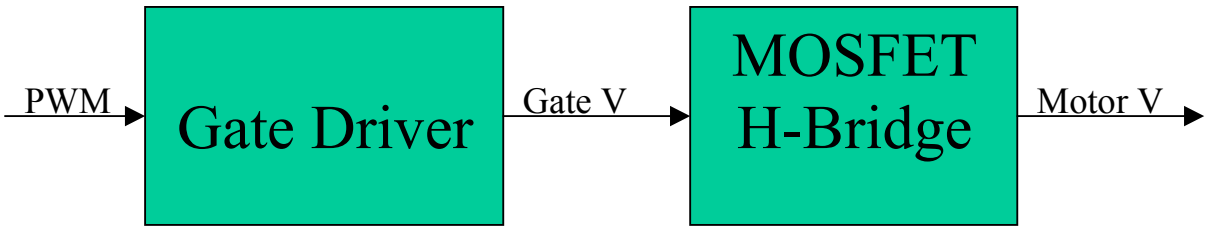



*Figure 15: Block Diagram of the Motor Drivers*

As shown in the block diagram above there is two main parts to the semi-discrete solution, the gate drive circuitry and the MOSFET's forming the H-Bridge. The semi-discrete solution calls for an integrated gate driver to be selected. Therefore the two decisions to be made in this section is the choice of a driver chip and MOSFET's.

#### 4.5.1 MOSFET driver selection

MOS transistors turn on when a positive voltage is applied from the gate to the source of the device. For most devices the switching occurs when Vgs is above 2V-5V and the maximum value of Vgs is usually around 20V for a device in a 42V, 4A application. When the FET is

turned on the Vs rises until it reaches the value of Vg, if Vg is then not changed relative to Vs the device will switch off without waiting to be turned off and the bridge will not work effectively. To alleviate this problem the gate driver provides a bootstrap differential to vary Vg and allow the device to stay on when required. The driver chip should be able to control each leg of the bridge independently so that bipolar switching is not forced as well as being able to supply enough current to charge the G-S capacitance at switching frequencies up to 100kHz.

There were three main suppliers of gate drivers, ST, Intersil and International Rectifier. The majority of these were either built for 20V or 600V systems. The devices made for a 600V system would be appropriate for use in GUROO. The IR devices, for example the IR2104S have some very small package options with little external circuitry required, there were not suitable as they could only source a maximum 130mA which would just be enough to switch the FET's at 100kHz. The best option from the devices that satisfied the requirements was the HIP4081AIP from Intersil. Kennedy used this device in his PUMA arm control thesis in 1999 [5]. It is ideal for this situation as its four independent inputs allow full control of the bridge if required, it has adjustable dead-band and is more than capable of switching the FET's that would be selected. The 4081 does have some disadvantages due to its large package size and number of external components required.

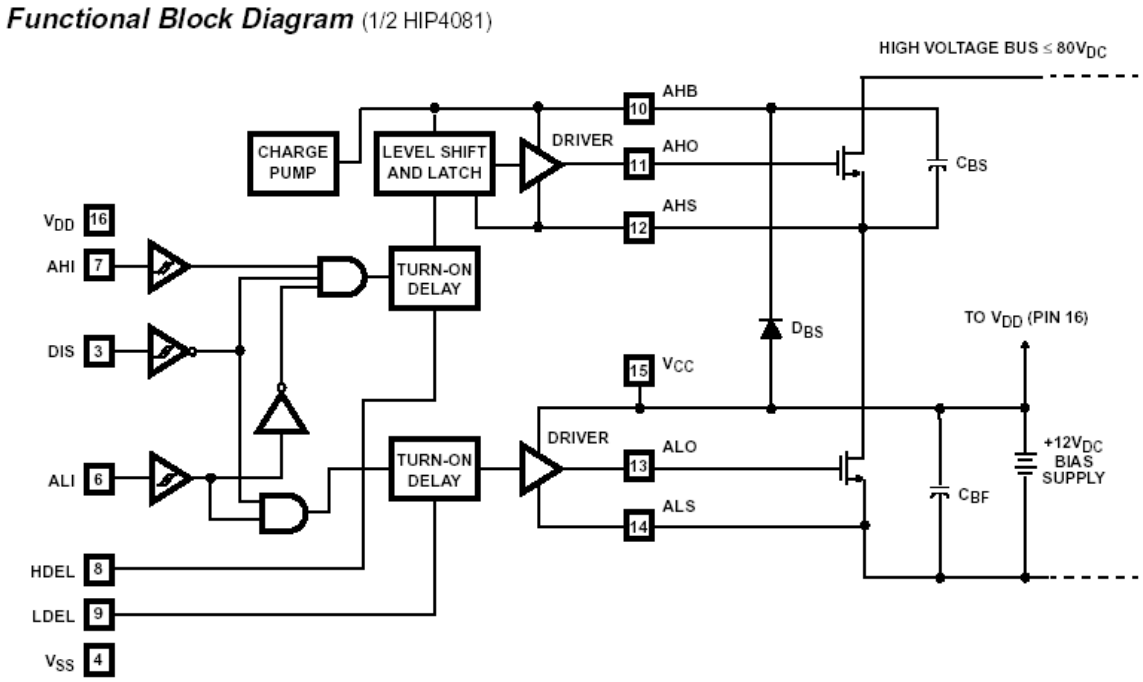



*Figure 16: HIP4081 Internal Block Diagram [10]*

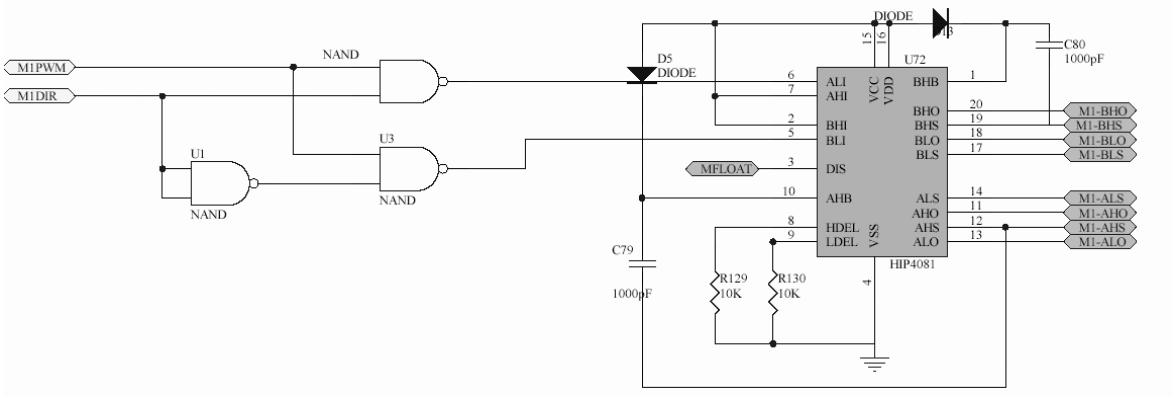



*Figure 17: HIP4081 Circuit Schematic*

### 4.5.2 MOSFET selection

The main reason to change from the integrated design used in the current boards to a semi-discrete solution was to improve efficiency. This improvement will depend on the FET's selected. The selection of the MOSFET's and a theoretical calculation of the power dissipation in the devices will now be discussed.

The main requirement of the FET's is to have a low Ron, be able to block 60V pulses as well as avalanche current. International Rectifier has a series of FET's to satisfy the power levels seen in this situation. The IRFZ44NS was the device selected, it has the lowest Ron of the series at 0.0165 Ohms and a reverse breakdown voltage of 60V. The FET selected is the N-channel device, as the matching P-channel FET has a much higher Ron it was decided to use N-channel devices in the top and bottom of the bridge.

*Figure 18: IRFZ44NS*

### 4.5.3 Power Dissipation

To ensure that the semi-discrete design would in fact increase the efficiency of power supply to the motors the levels of both switching and conduction losses were calculated. All MOSFET characteristics used in the calculations were obtained from the IRFZ44NS datasheet [11]. The losses were calculated as a worst case with a current of 4A being drawn through the device. A maximum supply voltage of 42V is assumed.

Conduction Losses:

When the device is turned on, there will be $I^2R$ losses present. In a device switching at 100kHz, as these FET's are expected to, the conduction losses are only a small component of the total power dissipation.

$$P = I^2 \times Ron$$

In the IRFZ44 I = 4A peak

And Ron = 0.0165 Ohms

$= 16 \times 0.0165$

$= 0.264\ W$ of conduction loss through one device

Switching Losses:

When a FET is switched there is large instantaneous power dissipation during the turn-on and turn-off intervals and this power can be estimated for each cycle as:

$$Pc = 0.5VdIoFs(tc\ (on) + tc\ (off))$$

For the device chosen:

Vd = 42 V

Io = 4 A

Fs = 100kHz; this is an anticipated value of the switching frequency

tc (on) = 110ns

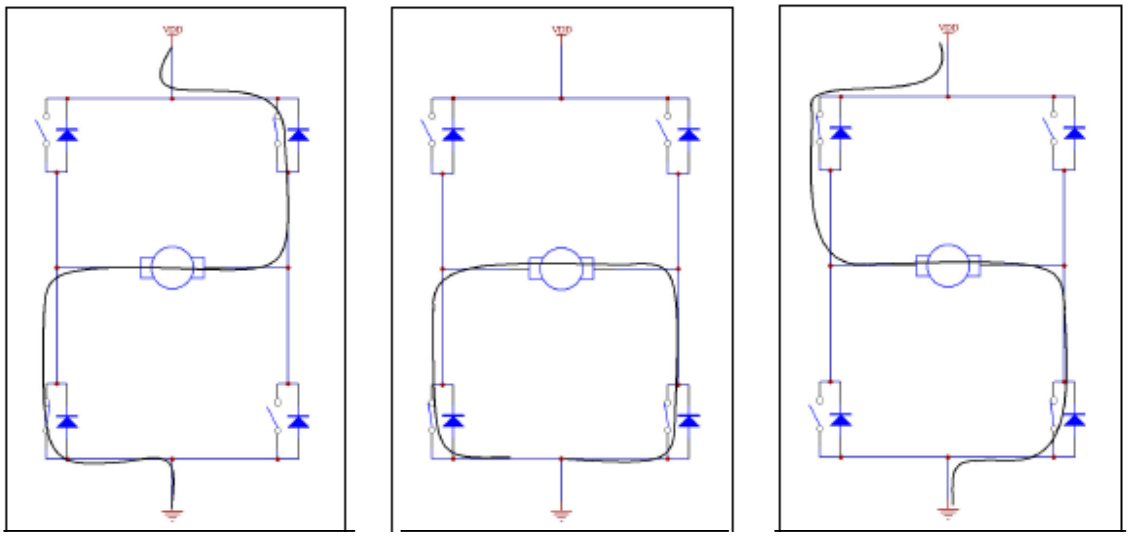
tc (off) = 137ns; t values from the IRFZ44 datasheet

$$Ps = 0.5 \times 42 \times 4 \times 100k \times (110n + 137n)$$
$$= 2.075\ W$$

The calculated loss through each device will be Ps + Pc, which is 2.339 W. As the maximum power dissipation to the PCB through the $D^2$ pack is 2 W the calculated value is slightly higher. This can be accepted as the power loss calculated is for a current of 4A, this value of current would not be seen for long periods of time, if at all. To further increase power dissipation the FET's could be mounted on the bottom of the board and placed against the frame of GUROO, this would supply the devices with ready-made heatsinks that would dissipate well in excess of the power levels calculated.

### 4.6 Current Sensing and Motor Protection

To allow the CPU to always have an accurate value of current being drawn by the motors, the current system of having a single sense resistor between the lower switches in the H-Bridge and ground will not suffice. As previously explained, the one-phase chopping method of switching uses three of the available four states of the H-Bridge.



*1. Motor running Forward* *2. Motor Braked* *3. Motor Running in Reverse*

*Figure 19: States of the H-Bridge used in One-Phase Chopping (Current flow)*

In the figure shown above, state 2: motor braked does not require any current to flow to ground. If the system of current sensing on the 2001 board was kept, the current flowing through the sense resistor would be zero and the CPU would register zero current flowing through the motor. It can be seen that this is not the case; there is a circulating current that must be accounted for when using one-phase chopping. By placing two sense resistors in series with the source's of the FET's and ground, the level of current flowing through each leg of the H-Bridge can be sensed and an accurate value for the motor current can be obtained at all times. As in the previous designs the voltage across these sense resistors is low pass filtered to remove switching noise and amplified to increase the accuracy of the reading from the processor's ADC. As there are now two current readings for each motor, the MC68376 will need to subtract the value over the second resistor before calculating the current. The value

must be subtracted as the current is flowing in the opposite direction in the second leg of the H-Bridge and therefore gives a negative voltage across the sense resistor. When the voltages over the resistors are subtracted, the polarity of the difference gives current flow direction. As far as motor protection goes, the processor is continually monitoring the motor current and a limit will be implemented in software that reduces the power supplied to the motor when this current reaches a prescribed value (nominally 4A). To further ensure the protection of the high quality (expensive!) motors, a hardware system was implemented to complement the fusing already present. Based upon Hood's design in 2002 a comparator is placed between a potentiometer and the output of the op-amp. The potentiometer is set to a voltage corresponding to the maximum allowable level of current and when the sense resistor voltage exceeds the potentiometer value, the comparator is set low and triggers an interrupt on the CPU. When the interrupt is called it will set the DISABLE pin of the MOSFET driver high and will turn all MOSFET's off, floating the motor.

### 4.6.1 Calculation of Component Values

The sense resistors should have a value as large as possible, to increase resolution and small enough to handle the currents flowing in the bridge. A value of 0.022 Ohms was selected for the sense resistors and this value is used as the starting point for the calculation of component values. When a current of 4A is flowing the power dissipated in the resistor is:

$$\begin{aligned} Pr &= VI \\ &= 88mV.\ 4A \\ &= 0.352\ W \end{aligned}$$

If a 1W resistor is chosen, there is no problem with exceeding the power rating.
The low pass filter placed after the sense resistor eliminates switching noise from the FET's to ensure the switching is not measured, Fs << Fc, where Fc is the cutoff frequency of the filter. Choose to set Fc = 1/10 of Fs, therefore Fc = 10kHz.

$Fc = 1 / 2\Pi RC$ choose a value of 100pF for C

$10k = 1/ 2\Pi R \times 100p$

$R = 150k\ Ohms$

The filtered signal then must be amplified to a maximum of 5V to be input into the ADC. Using a maximum current of 4A, the voltage across the sense resistor:

$V = I R$

$= 0.088\ V$

To set this to 5V requires a gain of approximately 57. To calculate the resistor values for the amplifier:

$Av = 1 + R2/R1$

$R2 = 56 \times R1$

Choose R2 = 150k Ohms

R1 = 2.7k Ohms this gives a gain of 55.5 which is appropriate.

The two chips required for this part of the design, a comparator and an op-amp were selected on the basis of package size and 5V operation. No special requirements were needed, so the standard devices used on the existing boards were used to start the selection process:

- LM2901 Comparator was chosen as it works to specification on the current boards and has been reliable in use, so there is no requirement to change the device.

- LM339 Op-amp has been selected to complete the voltage comparison between the amplified value and the potentiometer voltage. The 339 has been selected for its open-collector output which will eliminate the need for the external logic on the 2001 boards and greatly simplify the current sense circuitry. The open-collector devices do however have a much larger propagation delay than other designs with a value of 500ns compared to 4.5ns. It was decided that any value less than 1us would be acceptable.

According to calculations completed by Hood [7] this value of propagation delay along with slew rate of the op-amp and the delay in the processor would allow a rise of 0.14A above the value set in the potentiometer. This value was considered acceptable as it is well below a level that would cause damage to the motors or other circuitry.

### 4.7 Power Supply

Following the specifications outlined in the previous section, the power supply for the new design consists of two buck converters cascaded to regulate the 42V supply to the 12V and 5V required by the controller circuitry. A block diagram is shown below:

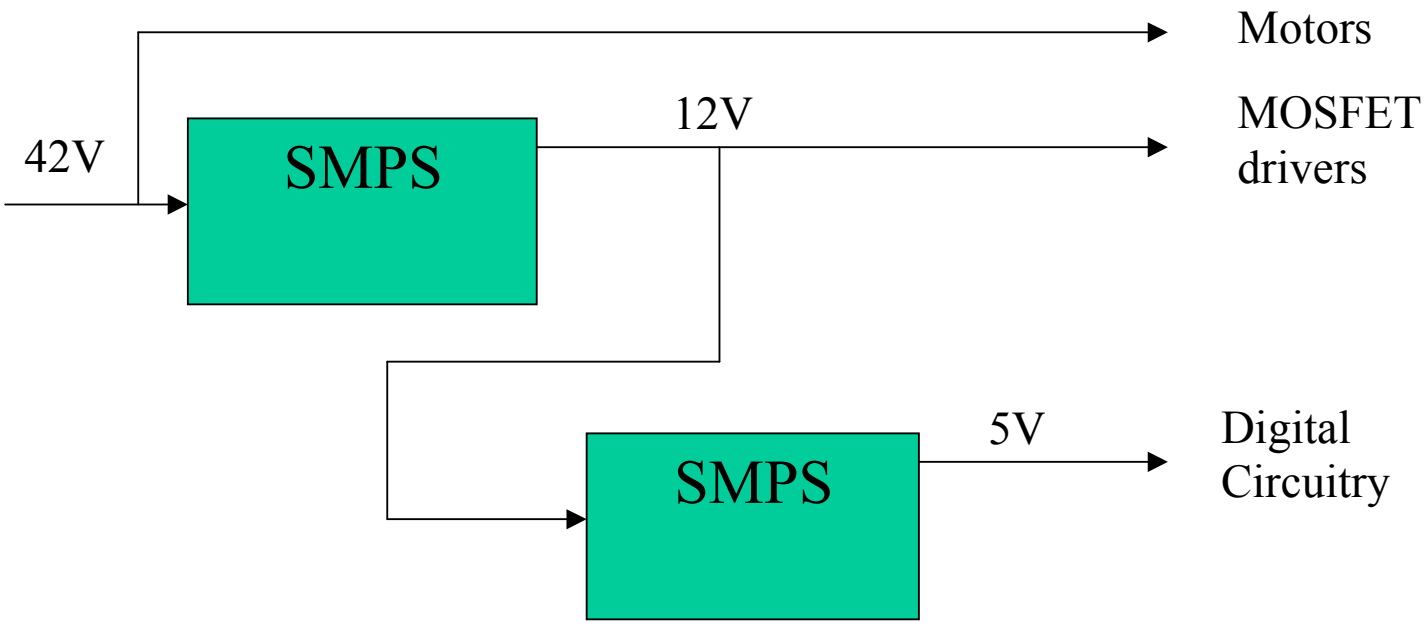



*Figure 20: Block Diagram of the Power Supply*

The switch-mode power supplies can be implemented in one of two ways:

1. A semi-discrete solution, consisting of a FET, output filtering and a controller chip e.g. TL494.
2. An integrated package where the switch is included with the controller.

As there is no advantage to using a semi-discrete solution, it only adds extra complication and components. It was decided to implement an integrated design for the power supply.

### 4.7.1 Buck Converter Selection

A number of chips were found that could fulfill the power supply specifications. Most of the devices were designed for use in telecommunications where the 48V on the telephone lines is regulated to the low values required at the user end, with an efficiency of close to 95%. Devices from MAXIM, National and Linear Technologies were considered and all had similar operating conditions. The LT1676 from Linear was chosen as it has the smallest number of external components, is voltage selectable and can supply up to 700mA with very small levels of output ripple. The converters current ratings have been estimated at:

| **Converter** | **42v to 12v** | **12v to 5v** |
|---|---|---|
| MC68376 | - | 300mA |
| HIP4081 | 100mA | - |
| Peripheral Chips | - | 100mA |
| Memory | - | 20mA |
| Current Sensing | 50mA | - |
| **Totals** | 150mA | 420mA |

*Table 2: Current Supply Estimates*

As the 42v – 12v converter must also supply the current to the 12v – 5v converter, the total current that needs to be supplied from the 12v output is:

*I = 150mA + 420mA. (5/12)* If the converter is assumed ideal

*= 325mA*

Which is under the maximum 700mA that the LT1676 can supply.

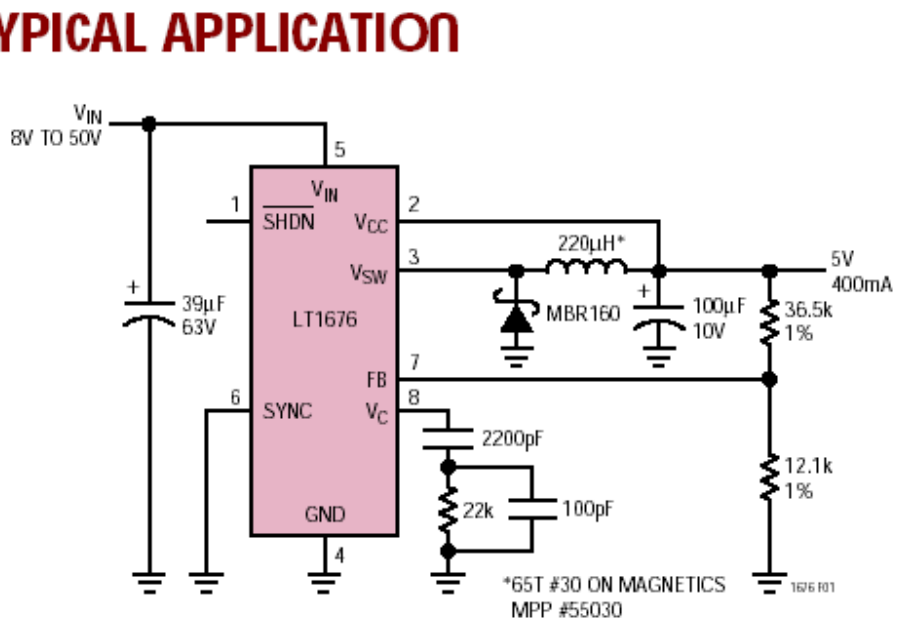



*Figure 21: Typical Application for a LT1676 (5v) [12]*

### 4.7.2 Calculation of Component Values

Output inductor selection using the following equation:

$$L = (Vo / f . Ipk). ((Vin-Vo)/Vin)$$

Ipk is from the internal set dV/dT threshold and is given as 200mA. F is the switching frequency and has been chosen at 100kHz to give reasonable output ripple levels.

For the 42v-12v converter:

$$L = (12 / 100k . 200m) . ((42 – 12)/42)$$
$$= 450uH$$

Choose the standard value of 470uH

For the 12v-5v converter

$$L = (5 / 100k . 200m) . ((12 – 5)/12)$$
$$= 146uH$$

Choose the standard value of 150uH

Using the peak current rating for the first converter of 325mA, need to rate the inductors for a minimum of 500mA.

Now select the by-pass capacitor values:

*C = 39uF for the input smoothing capacitor*

*C = 100uF for the output capacitor to allow for a low enough cutoff frequency for the low-pass output filter. This in turn eliminates any output voltage ripple.*

Select the diodes to allow the current to flow out of the inductor:

*Choose a Schottky diode rated at 20V, avoid using an ultra-fast device.*

Select a ratio of the voltage divider to set the reference voltage, as the non-inverting input of the reference amplifier is tied to 1.24V, the Vref input must be equal to 1.24V when the output is at its required value.
For the 42v – 12v converter:

*1.24v = (Vo . R2) / (R1 + R2)* *Let R2 = 12k Ohms*
*R1 = 104k Ohms*

For the 12v – 5v converter:

*1.24v = (Vo . R2) / (R1 + R2)* *Let R2 = 12k Ohms*
*R1 = 36k Ohms*

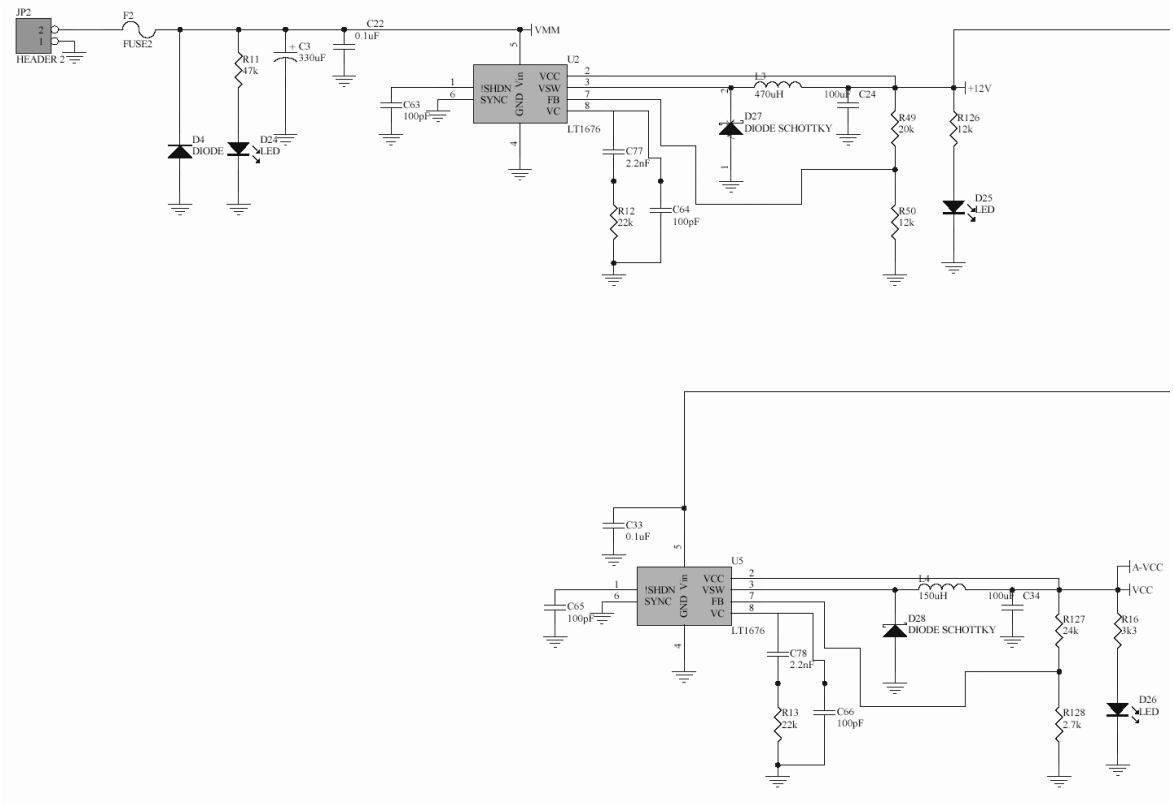



*Figure 22: Power Supply Schematic*

### 4.8 Joint Alignment Sensing

In Andrew Hood's thesis in 2002, a system for aligning the joints at start-up was proposed using an optical alignment board and infrared LED's. After calculating the maximum error seen when using the encoder index pulse as an alignment indicator, the result was 2 degrees. This level of error was acceptable and there was no need to integrate a separate alignment system into the new design.

### 4.9 Peripheral Device Selection

The selection of the peripheral devices was relatively straightforward due to lack of choice and the fact that the chips used on the 2001 boards work effectively.

**CAN**

Very few CAN transceivers exist, maybe due to the fact that it is a new and not widely used system. Maxim, TI and Philips manufacture devices that would fulfill the requirements, but it was decided to stick with the Philips PCA82C250 that is currently used on GUROO. There have been no problems with the Philips chip and it has exactly the same pin-out as all the other devices, so there was no reason to change from what is known.

**SCI**

When selecting an SCI transceiver, the MAX3221 was chosen as it is based upon one of the most widely available and cheapest devices, the MAX323. It exceeds the 323 by having an enable and an invalid function, allowing more accurate monitoring of the serial data.

**Reset Chip**

The reset chip holds the reset line of the processor low for a period of time when the device is first powered up. The reason for doing so is twofold:

1. Filter out the de-bounce from the reset button.
2. Protect the processor from the slow voltage increase on the power rail to ensure reliable start-up conditions.

The 811 holds the reset line low for 150ms after power-up and this time is appropriate for the MC68376. The MAX811 is a commonly used device for this application and has been used on the 2001 boards, there was no need seen to change from this cheap and reliable device for the new design.

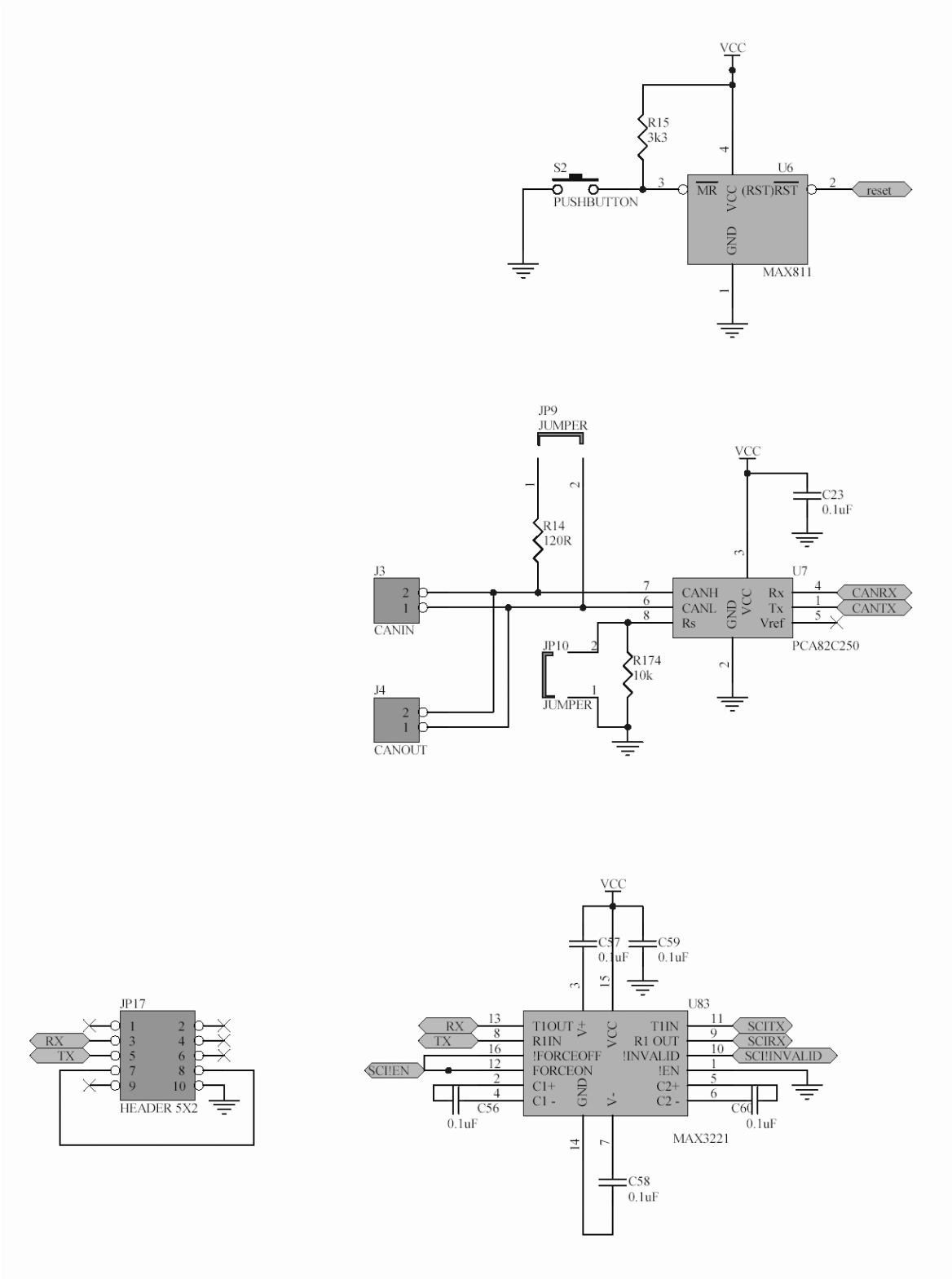



*Figure 23: Peripheral Device Schematic*

# 5. Testing Results

Whilst completing the new design a test board was constructed to test the operation of the new H-Bridge and current sensing circuits. This section will outline the tests carried out and the results obtained. The main goal of the new motor drive circuitry was to reduce power dissipation in the system, and therefore the main goal of the testing was to verify the values calculated in the previous section.

### 5.1 Test Circuitry

The test board consisted of the H-Bridge, MOSFET driver and the current sense circuitry. No external logic was included so each leg of the bridge could be independently controlled. The 20-pin DIP version of the HIP4081 was used in the testing stage, as it was readily available from the regular suppliers and allowed the pin conditions to be easily supervised. The rest of the circuitry is identical to the components chosen in the previous sections.

| Component | No. | Manufacturers Code |
|---|---|---|
| Schottky Diodes | 2 | HSMS-2800 |
| MOSFET Driver | 1 | HIP4081AIP |
| 5A fuse | 1 | 303-0143 |
| Comparator | 1 | LM339M |
| Op-Amp | 1 | MAX4168EPD |
| MOSFET's | 4 | IRFZ44NS |
| Sense Resistors | 2 | OR22 |
| S.M Capacitors | 5 | Various |
| S.M Resistors | 9 | Various |
| 330uF Electrolytic Cap | 1 | 320-1612 |
| Potentiometer | 1 | 988-273 |

*Table 3: Test Board Components*

It was decided to build the test circuitry on a PCB, as the currents present in the H-Bridge would be too high for breadboard. The PCB was routed with easy attachment of test equipment in mind and space was left between the devices to allow for CRO leads and the like to be connected.

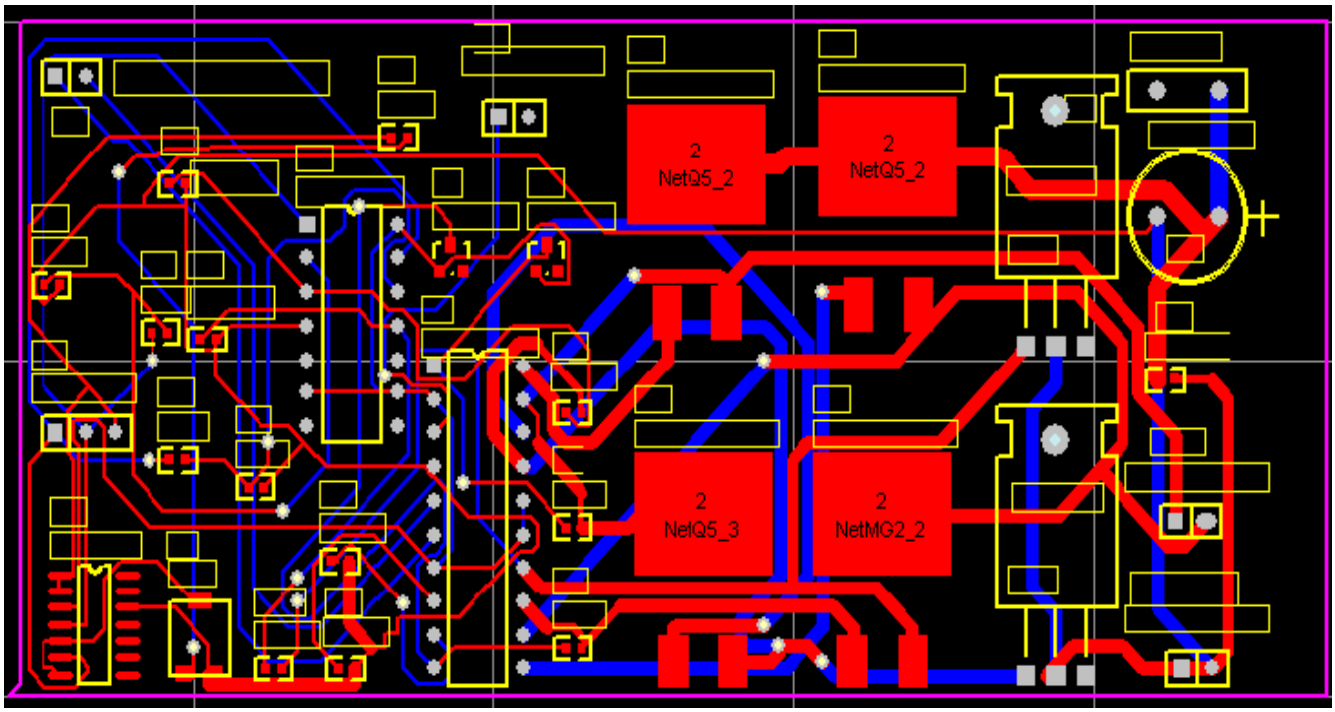



*Figure 24: Test Board PCB Layout*

The figure above shows the layout of the PCB, the 20-pin HIP chip can be seen in the center of the figure. To the right is the 4-MOSFET H-Bridge with the larger tracks to accommodate the 4A peak current that will be seen in this side of the board. To the left is the current sense circuitry, consisting of the op-amp, comparator and potentiometer.

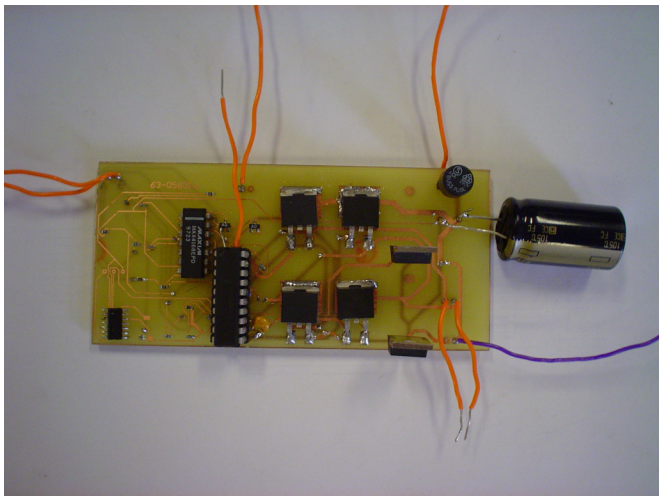


*Figure 25: Motor Drive Test Board*

**5.2 Motor Drive Testing**

To test the motor circuitry the board shown above was first connected with an open circuit load at the motor terminals. This was to ensure the HIP device was responding correctly to the inputs and that no shoot-through or other damaging effects were present. Once the operation of the circuit was verified and one small bug repaired, (pins 12 and 13 of the HIP were incorrectly swapped on the PCB footprint) the open circuit was replaced with a load. As a motor was not available for use in testing as one of GUROO's joints would have to be disassembled to enable the motor to be removed. To accurately model a DC motor an inductor and a resistor must be connected in series. Looking at the datasheet of the motors and using readily available components the closest match to a real motor was a 1-Ohm 25W resistor and one of the inductors used on GUROO to reduce the ripple current. The 1-Ohm resistor was chosen to enable high levels of current to be generated from a lower voltage, which could be supplied by regular lab power supplies. The components used are shown below:

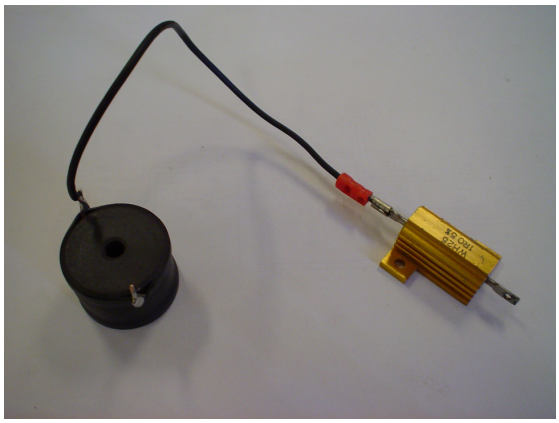


*Figure 26: Simulated motor load*

The inputs of the HIP4081 were driven using a signal generator to model the PWM output of the processor, when testing one input was held low while the other was driven with the S.G, to model the external logic on the complete design.

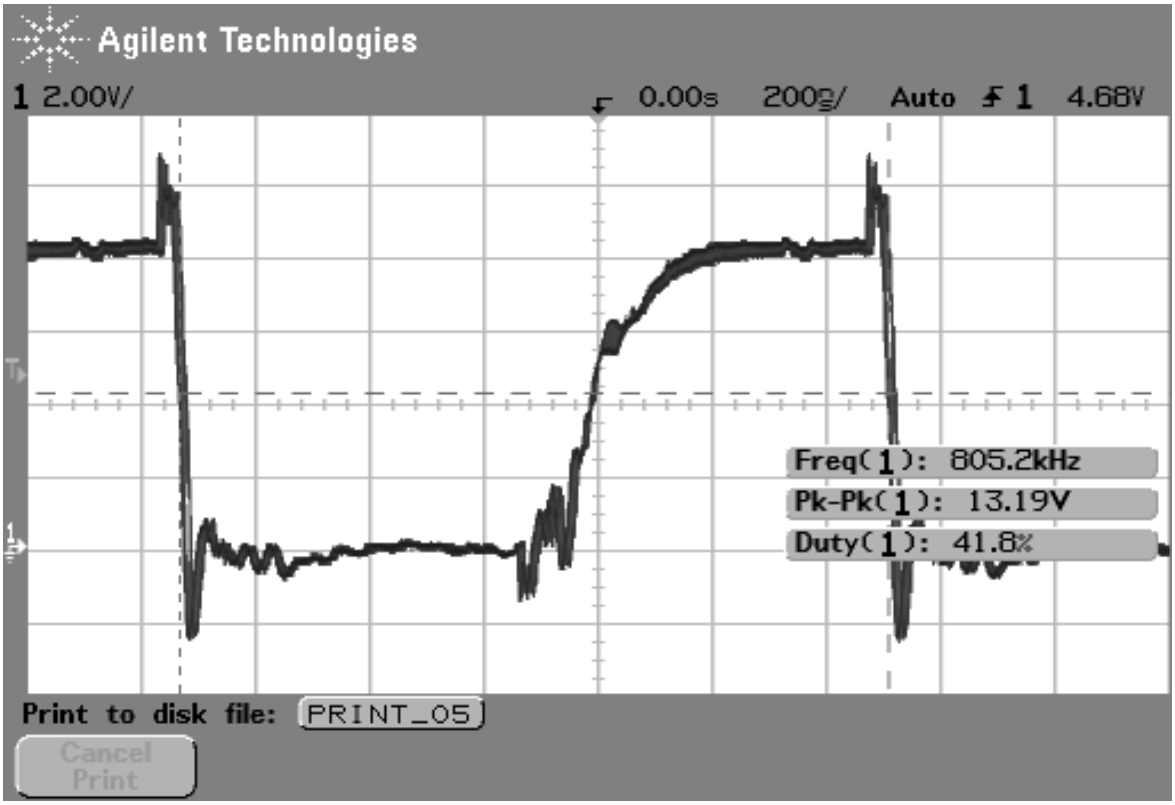



*Figure 27: Distorted waveform at 800kHz*

Firstly the driver was input with frequencies ranging from 100kHz to 1Mhz, the rated maximum of the device. This maximum would not be suitable for switching the FET's in this circuit as the waveform became quite distorted as the frequency was raised over 400kHz. The slow rise and fall times present at these high frequencies would increase the switching losses up to 10-12W, much larger than is possible to dissipate without heatsinking (see figure above). As the switching frequency in the design has been chosen at 100kHz, this distortion should not be a problem.

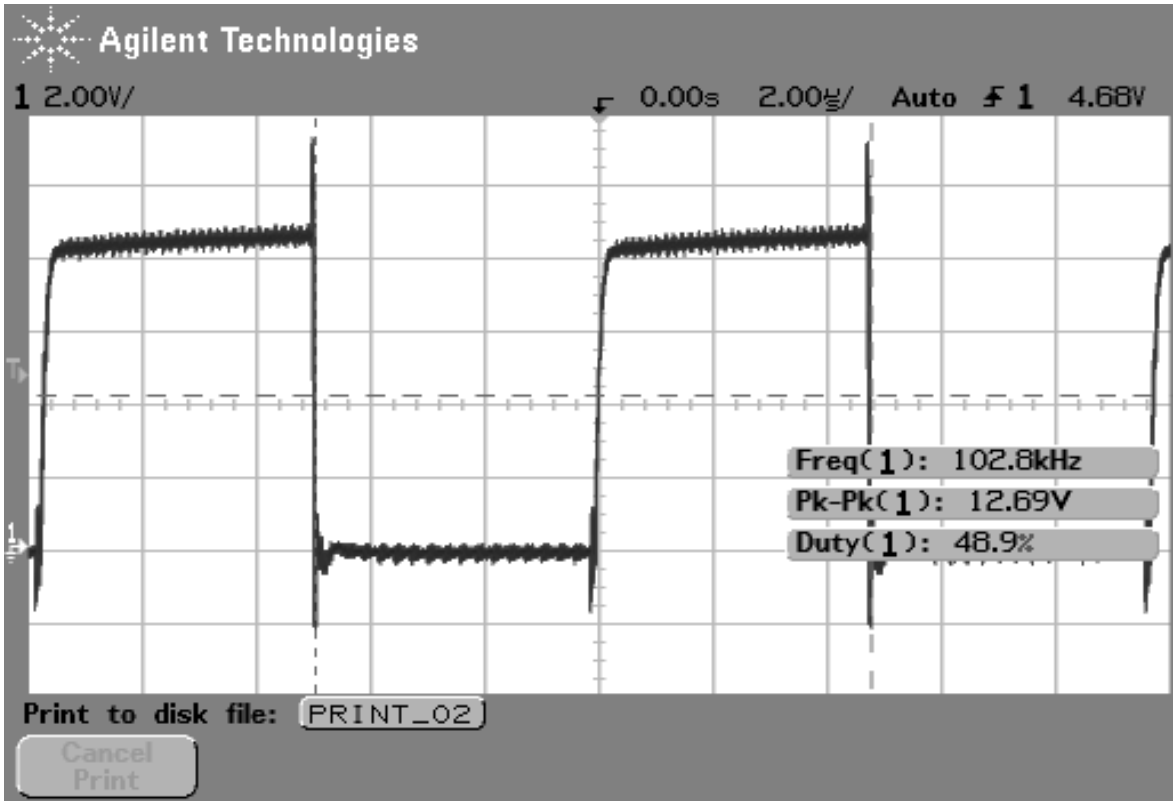



*Figure 28: Voltage across the load with 50% duty, 12.69V pk-pk at 102.8kHz*

The rise and fall times of the FET's were observed at 200ns and 140ns respectively when switching at 100kHz. These values are slightly larger than the values given by the MOSFET datasheet and used in the power dissipation calculations. If the calculations are repeated with the observed switching times, the losses become:

$$P = 0.5\ V\ .\ I\ x\ (tr + tf\ /\ T)$$
$$= 2.857\ W$$

This value of power loss is considerable and is larger than what the devices are rated to dissipate. In the final design some means of heatsinking will be necessary. The probability of a sustained 4A current is low, but must be considered for in the calculations. In the oscilloscope printout shown above a large occurrence of ringing can be seen, this phenomena should not affect the operation of the motors and may be damped out if the motors are loaded.

### 5.3 Current Sensing Testing

The current sensing circuitry was included on the test board and worked to expectation in all the motor drive tests outlined above. The current sensing system is very similar to the design used on the 2001 boards, so a discussion of the specification of the circuitry is not required here. The new part of the design, adding a potentiometer to dial in a current limit was seen to not really be necessary as a resistor of the required value would give just as accurate results and the value of the maximum current could easily be figured out. If the potentiometer was used, the value could be changed by mistake or the value lost when tuning occurs without appropriate documentation. In the complete design the potentiometer was left in, so the constructor of the boards can make the decision on whether to include the component or to use a fixed value resistor in its place.

### 5.4 Testing Conclusions

The test board was used as verification for the power dissipation calculated in earlier sections and it was found that the actual power dissipated in the MOSFET's is slightly larger than those calculated. The contributing factors to the difference are the delay through the driver chip, losses in the too small PCB tracks and differences between the load used for testing and the actual values of the motor used in the calculations. The results obtained during testing supports the need for a semi-discrete solution in the new design and proves the design calculated in earlier sections would lead to an improvement in performance from the motor drivers. The

current sensing system worked as expected and will be kept for the complete design, a modification concerning the use of the potentiometer may be considered when it comes time to construct the design.

# 6. Board Layout and Placement

## 6.1 Board Layout

As the new design allows five motors to be controlled per board, three boards will be required to control the high power lower body motors and one board to control the upper body servomotors. The PCB's will have a general layout as shown:

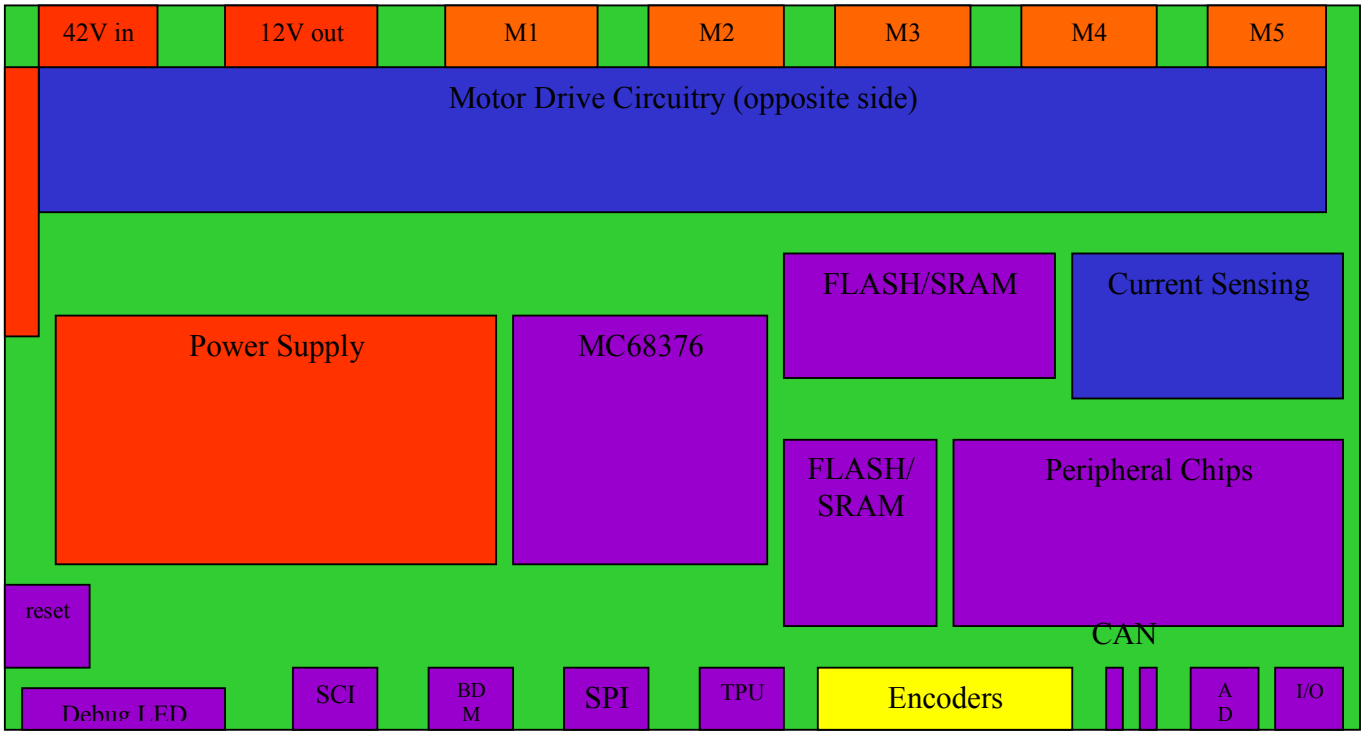



*Figure 29: Controller Board Layout*

Where: Red = Power

Blue = Motor Drive and Current Sensing

Purple = Digital Circuitry

Orange = Motor Power Connectors

Yellow = Encoder Connectors

The connectors marked TPU, A/D and I/O are headers taken directly from spare pins on the CPU, they are for connection of extra devices if required by future needs.

### 6.2 Connectors

The data connectors have been chosen to be standard locking IDC headers. The motor power, 42V in, and 12V out will all be Molex Mini-fit Junior Power connectors, available from RS components (order no. 215-5815). These connectors allow for simple connection, can handle the high currents and can be daisy-chained to reduce wiring.

### 6.3 Placement

Due to the great reduction of the number of boards in the lower body, the placement into GUROO can be a little more subtle than the current arrangement where there is a mass of wiring and PCB's present. The boards will be placed as far out of sight as possible while still allowing debugging to take place. To allow the MOSFET's to operate without heatsinking, it has been decided to mount the FET's and HIP4081's on the reverse of the boards. By adding some heat conducting paste and pressing against GUROO's frame it should be possible to dissipate well over the 2W expected. As only two pairs of wires will be required to connect the boards, (CAN and 42V) wiring the boards together should be relatively straightforward. The orientation of the boards will be important, the long side with the digital connectors should be placed to the outside, allowing the LED's to be easily seen and the processing monitored. The opposite side with the motor and power connectors can be hidden as they should not need to be accessed once the boards are installed. The two boards controlling all of the lower leg and part of the hip will be mounted against the back of the thigh, the perforated aluminium sheets on GUROO's thighs at present will be replaced with solid sheets and the boards mounted onto these. The area is shown in the picture below by the green rectangles in the top thigh, due to the smaller number of boards used, the bottom of the leg will be free from electronics.

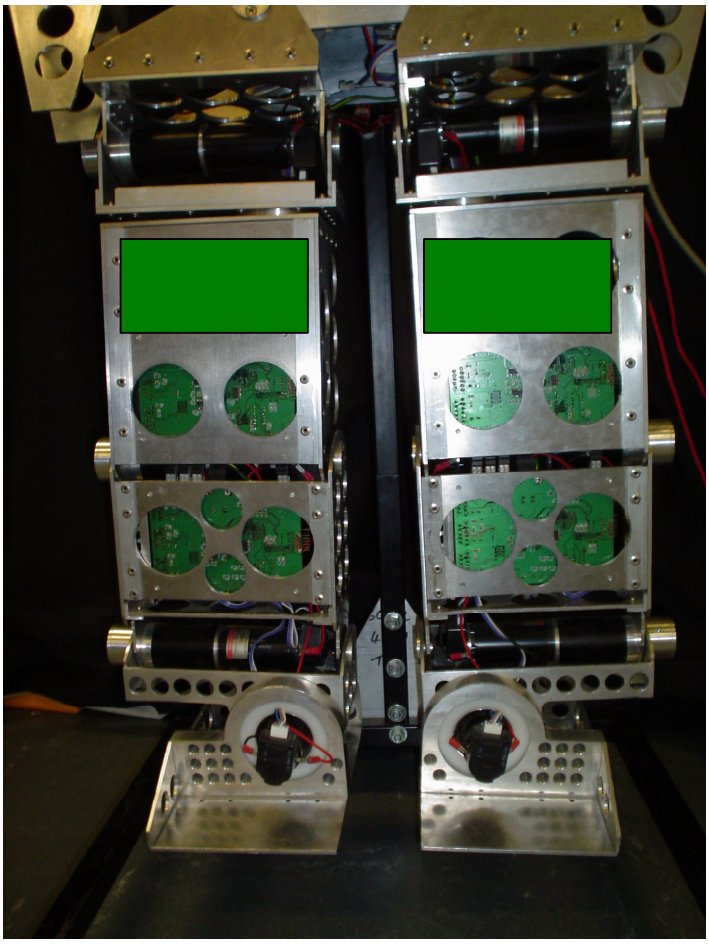


*Figure 30: Front view of GUROO's legs where two of the new boards will be placed (shown in green)*

One other board will be required to control the upper DC motors present in the torso. The board will be placed in the same position as one of the current boards, in the lower torso. This position is well hidden but also allows access from underneath for debugging and maintenance. This position is shown in the picture of the current board:

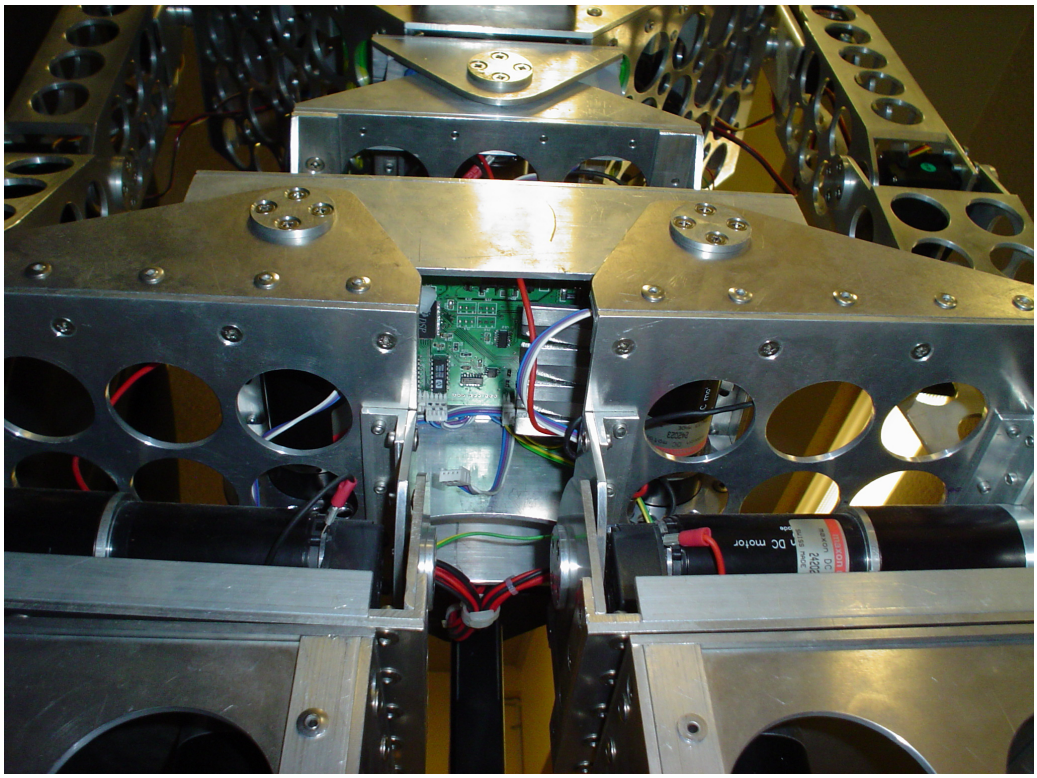


*Figure 31: Position of hip controller*

# 7. Project Conclusions

At the start of the project the original goal was to produce a set of working distributed controller boards for integration into GUROO. As the project progressed, testing was needed to be sure of the performance of the design and the goal was changed to producing a well thought through and tested design. During the last week of October, the design will be handed over to Damien Kee and it is planned the PCB routing and construction of the boards will be completed by early 2004. The design was completed in parallel with a new hardware design for the ROBOROO's and most of the digital design has been standardised between the teams. This homogenization will allow the two UQ robotics teams to work together and share development tools, benefiting both parties. The new hardware design, when completed, will allow GUROO the chance to run to his full potential without the burden of the unreliable and often damaged version 1 of the hardware.

# 8. Future Work

In order to have the design proposed in this thesis integrated into GUROO, the following work is still to be completed:

- The PCB layout and routing must be completed, along with verification that the components chosen will still be available when the boards are to be constructed.
- Construction and circuit verification of the boards.
- The control loop software will need to be adapted to run on the new processors.
- Design of the servo motor board, involving a modification to the power circuitry of the design proposed in this thesis.

# 9. References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9. Motorola, *MC68376 Datasheet*, Revised 15 October 2000
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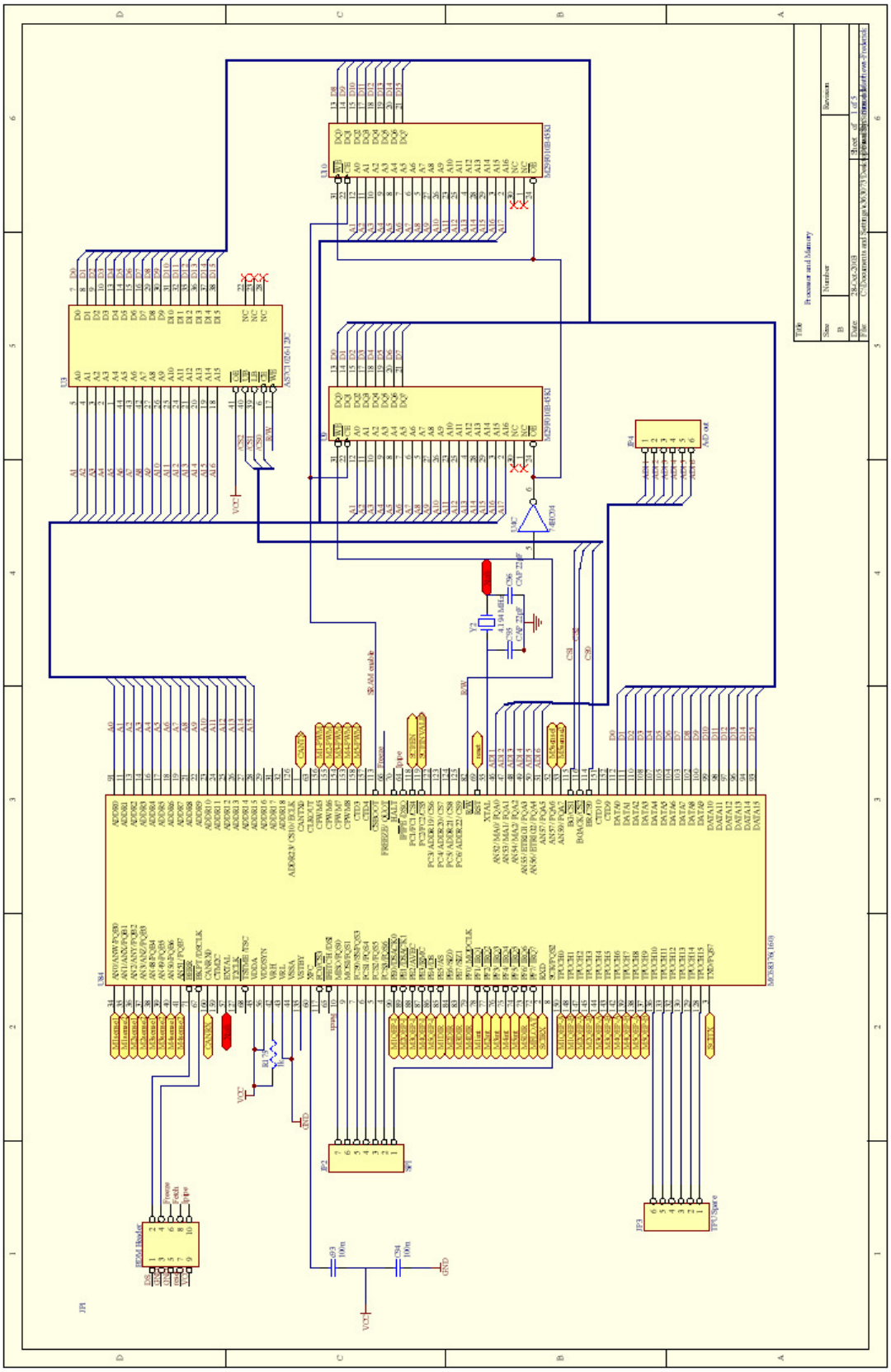
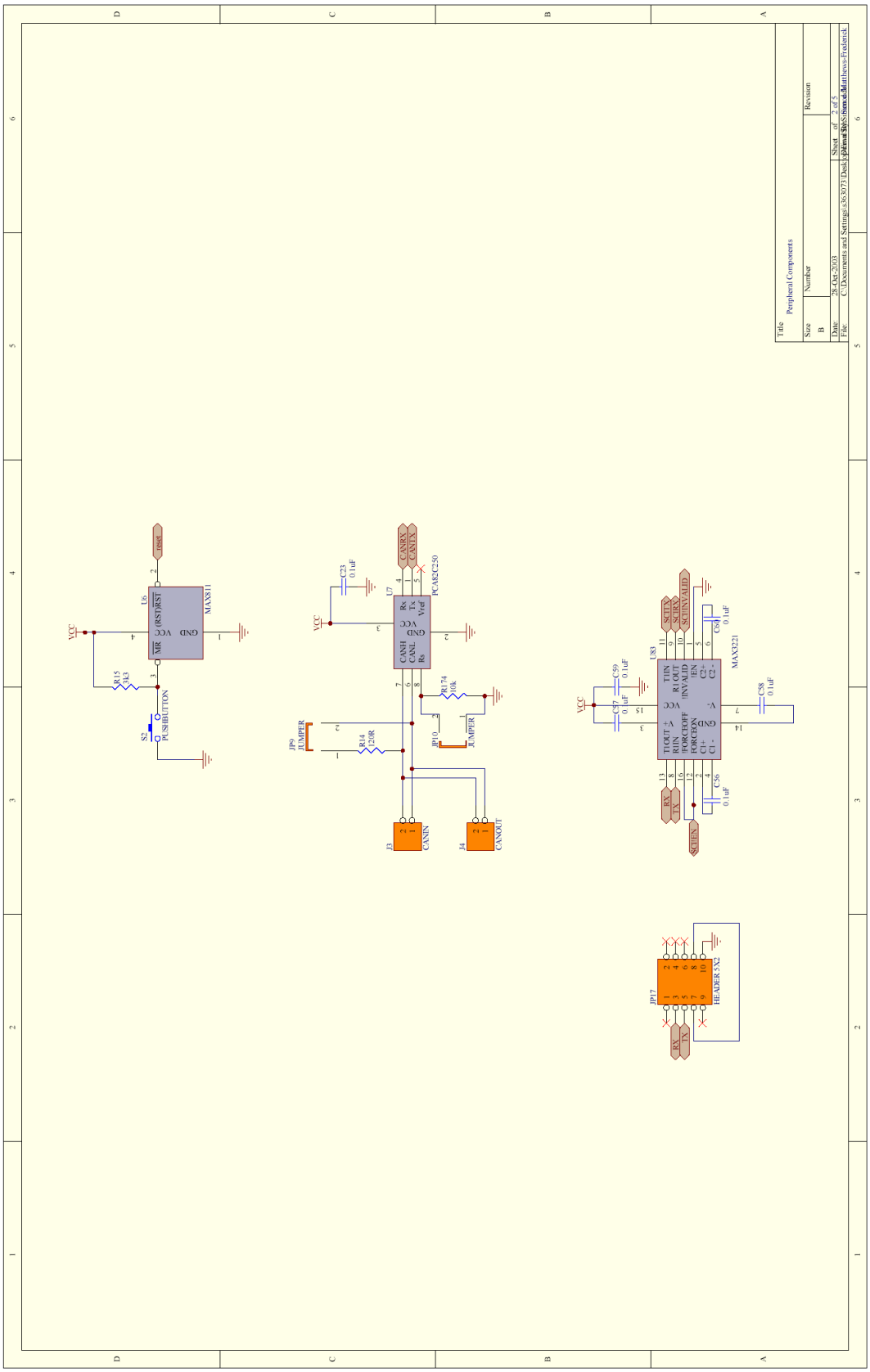
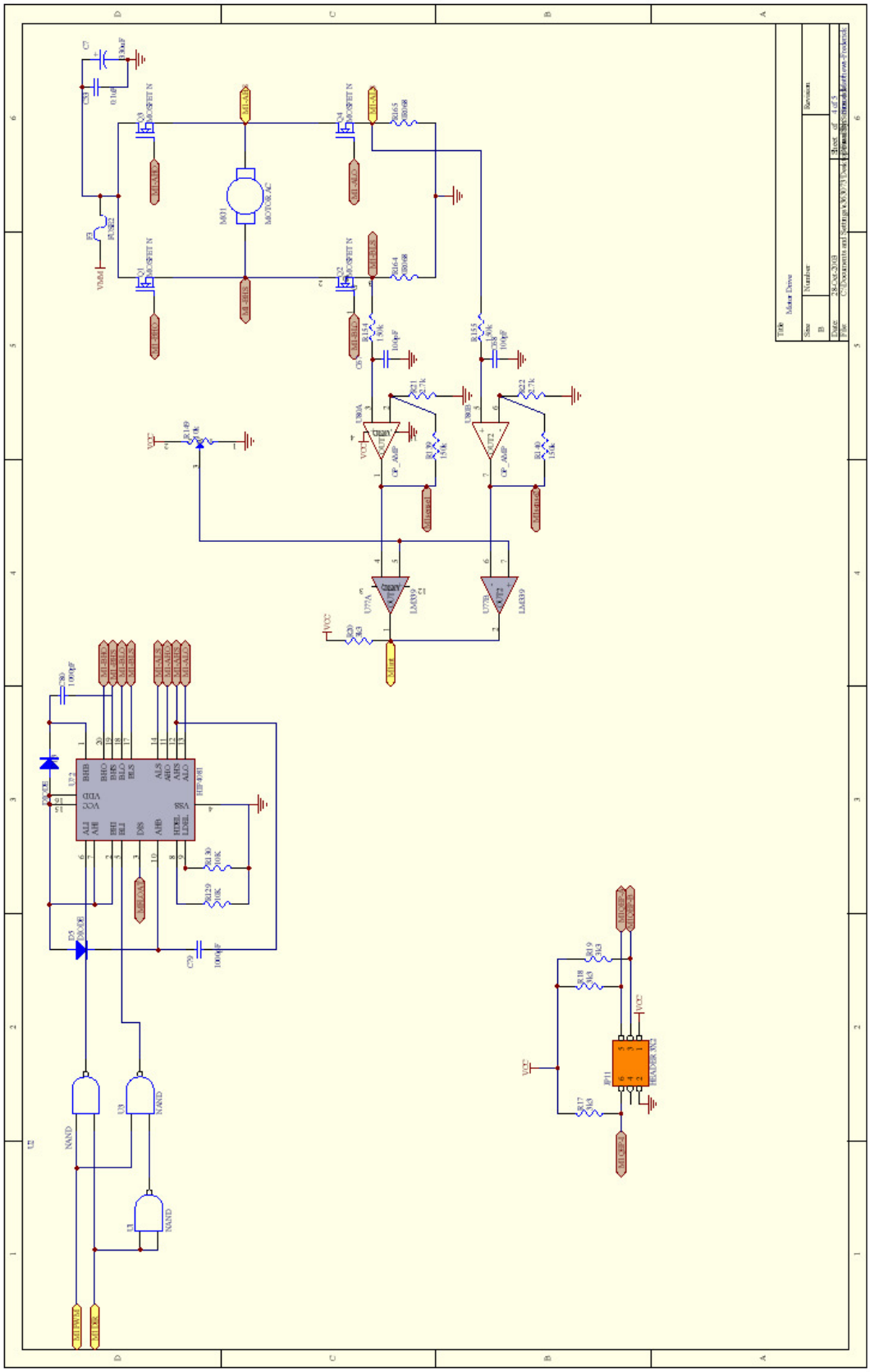
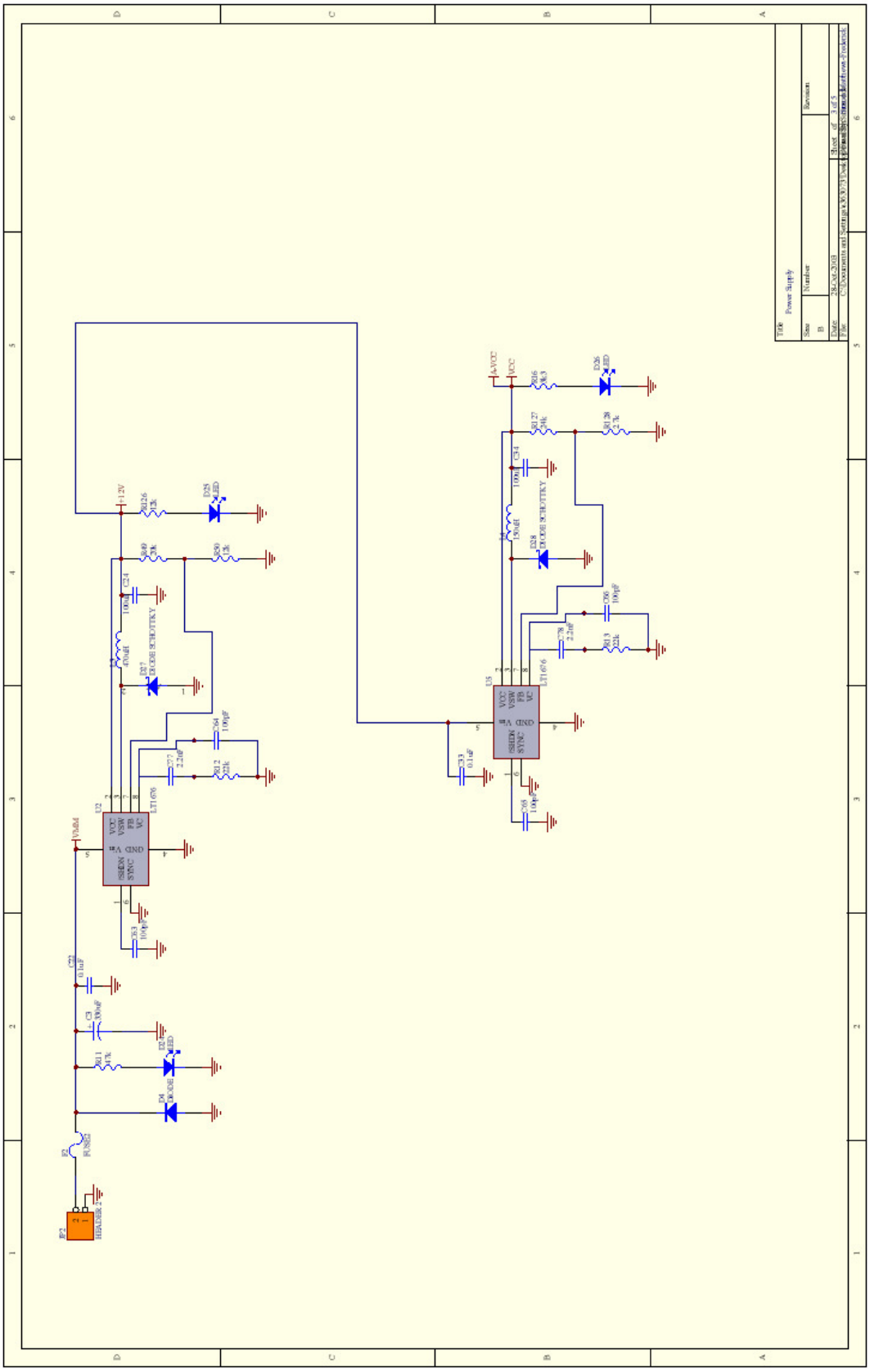
11. International Rectifier, *IRFZ44NS Datasheet*, 13 March 2001
12. Linear Technologies, *LT1676 Application Notes*, 1998
13. ST, *M29F010B Flash Datasheet*, April 2002
14. Alliance Semiconductor, *AS7C31026 SRAM Datasheet*, March 2002

# Appendix A: New Design Schematics




Title
Peripheral Components
Size
B
Number
Revision
Date
28-Oct-2003
Sheet
2
of
5
File
C:\Documents and Settings\s36.9073\Desktop\Simon Matthews-Frederick
reset
U6
MAX811
(RST)RST
VCC
GND
MR
VCC
R15
1k3
S2
PUSHBUTTON
C23
0.1uF
U7
PCA82C250
CANRX
CANTX
Rx
Tx
Vref
CANH
CANL
Rs
R174
10k
JP9
JUMPER
R14
120R
JP10
JUMPER
J3
CANIN
J4
CANOUT
U83
MAX3221
T1OUT
R1IN
T1IN
R1 OUT
INVALID
FORCEOFF
FORCEON
EN
C1+
C1-
C2+
C2-
V+
V-
GND
SCITX
SCIRX
SCIINVALID
SCIEN
C59
0.1uF
C57
0.1uF
C60
0.1uF
C58
0.1uF
C56
0.1uF
JP17
HEADER 5X2
RX
TX





# Appendix B: Selected Datasheets

Figure 1: HIP4081AIP Datasheet

Figure 2: IRFZ44NS Datasheet

Figure 3: LT1676 Application Notes

# HIP4081A, 80V High Frequency H-Bridge Driver

**Application Note** **February 2003** **AN9405.4**

*Author: George E. Danz*

## Introduction

The HIP4081A is a member of the HIP408X family of High Frequency H-Bridge Driver ICs. A simplified application diagram of the HIP4081A IC is shown in Figure 1. The HIP408X family of H-Bridge driver ICs provide the ability to operate from 10VDC to 80VDC busses for driving H-Bridges, whose switch elements are comprised of power N-Channel MOSFETs. The HIP408X family, packaged in both 20 pin DIP and 20 pin SOIC DIPs, provide peak gate current drive of 2.5A. The HIP4081A includes undervoltage protection, which sends a continuous gate turn-off pulse to all gate outputs when the $V_{DD}$ voltage falls below a nominal 8.25V. The startup sequence of the HIP4081A is initiated when the $V_{DD}$ voltage returns above a nominal 8.75V. Of course, the DIS pin must be in the low state for the IC to be enabled. The startup sequence turns on both low side outputs, ALO and BLO, so that the bootstrap capacitors for both sides of the H-bridge can be fully charged. During this time the AHO and BHO gate outputs are held low continuously to insure that no shoot-through can occur during the nominal 400ns boot-strap refresh period. At the end of the boot strap refresh period the outputs respond normally to the state of the input control signals.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper halves of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to "maintain" bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin "float" along with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4081A can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. The HIP408X family of devices is fabricated using a proprietary Intersil IC process which allows this family to switch at frequencies over 250kHz. Therefore the HIP408X family is ideal for use in various high frequency converter applications, such as motor drives, switching power amplifiers, and high-performance DC-DC converters. A typical application is shown in Figure 5.

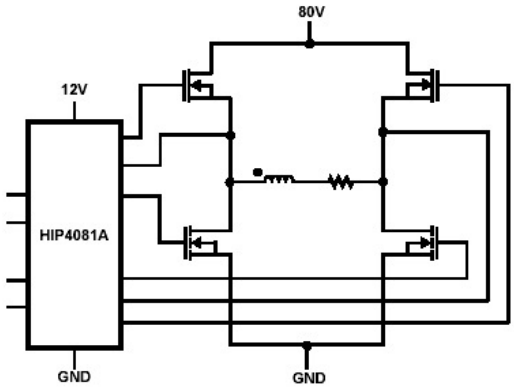



FIGURE 1. HIP4081A SIMPLIFIED APPLICATION DIAGRAM

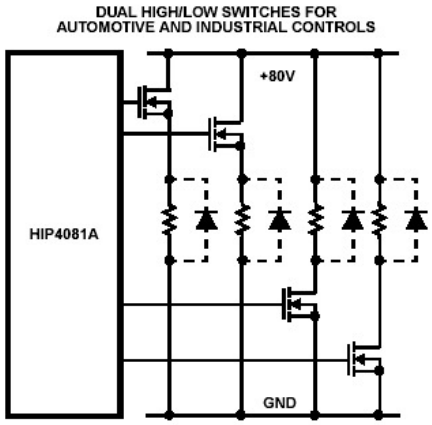



FIGURE 2. HIP4081A AS LAMP SWITCH DRIVER

To provide accurate dead-time control for shoot-through avoidance and duty-cycle maximization, two resistors tied to pins HDEL and LDEL provide precise delay matching of upper and lower propagation delays, which are typically only 55ns. The HIP4081A H-Bridge driver has enough voltage margin to meet all SELV (UL classification for operation at $\leq$ 42.0V) applications and most Automotive applications where "load dump" capability over 65V is required. This capability makes the HIP408X family a more cost-effective solution for driving N-Channel power MOSFETs than either discrete solutions or other solutions relying on transformer- or opto-coupling gate-drive techniques.

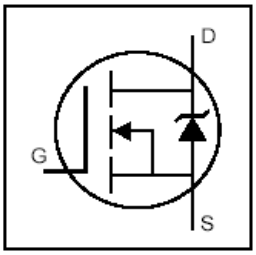
International
IOR Rectifier

PD - 94153

# IRFZ44NS
# IRFZ44NL

HEXFET® Power MOSFET

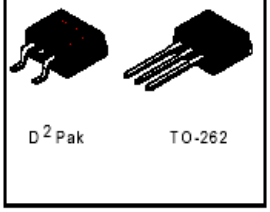
- Advanced Process Technology
- Surface Mount (IRFZ44NS)
- Low-profile through-hole (IRFZ44NL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated




$V_{DSS}$ = 55V

$R_{DS(on)}$ = 0.0175Ω

$I_D$ = 49A




## Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The $D^2Pak$ is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The $D^2Pak$ is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.
The through-hole version (IRFZ44NL) is available for low-profile applications.

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 49 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 35 | |
| $I_{DM}$ | Pulsed Drain Current ① | 160 | |
| $P_D$ @$T_A$ = 25°C | Power Dissipation | 3.8 | W |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 94 | W |
| | Linear Derating Factor | 0.63 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $I_{AR}$ | Avalanche Current① | 25 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | 9.4 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.0 | V/ns |
| $T_J$ | Operating Junction and | -55 to + 175 | °C |
| $T_{STG}$ | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | ---- | 1.5 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | ---- | 40 | |

LINEAR TECHNOLOGY

# LT1676

## Wide Input Range, High Efficiency, Step-Down Switching Regulator

## FEATURES

- **Wide Input Range: 7.4V to 60V**
- 700mA Peak Switch Current Rating
- **Adaptive Switch Drive Maintains Efficiency at High Load Without Pulse Skipping at Light Load**
- True Current Mode Control
- 100kHz Fixed Operating Frequency
- Synchronizable to 250kHz
- Low Supply Current in Shutdown: 30µA
- Available in 8-Pin SO and PDIP Packages

## APPLICATIONS

- Automotive DC/DC Converters
- Telecom 48V Step-Down Converters
- Cellular Phone Battery Charger Accessories
- IEEE 1394 Step-Down Converters

## DESCRIPTION

The LT®1676 is a wide input range, high efficiency Buck (step-down) switching regulator. The monolithic die includes all oscillator, control and protection circuitry. The part can accept input voltages as high as 60V and contains an output switch rated at 700mA peak current. Current mode control offers excellent dynamic input supply rejection and short-circuit protection.

The LT1676 contains several features to enhance efficiency. The internal control circuitry is normally powered via the $V_{CC}$ pin, thereby minimizing power drawn directly from the $V_{IN}$ supply (see Applications Information). The action of the LT1676 switch circuitry is also load dependent. At medium to high loads, the output switch circuitry maintains high rise time for good efficiency. At light loads, rise time is deliberately reduced to avoid pulse skipping behavior.

The available SO-8 package and 100kHz switching frequency allow for minimal PC board area requirements.



## TYPICAL APPLICATION

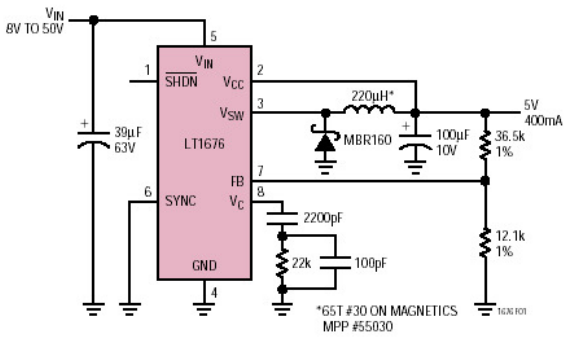
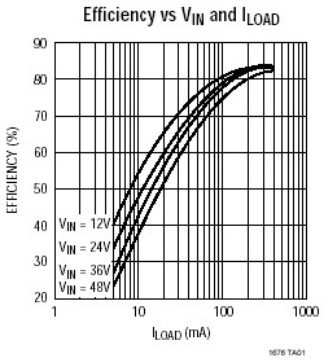



Figure 1



# Appendix C: Full Datasheets and Schematics

The CD attached contains a complete set of the datasheets used in the new design, as well as the final Schematic PROTEL database.