DATA SHEET

ET21x110C

32x32 sensor with 6 bit AD converter

Etoms Electronics Corp.

Office:
5F, No. 12, Innovation 1st. RD.,
Science-Based Industrial Park,
Hsin-Chu City, Taiwan, R.O.C
Tel: +886-3-6661766 ext.1672
Fax: +886-3-6661765

1. General description

The chip ET21x110C is a 32x32 sensor with high speed AD converter. It's convenient for motion detection and finger print checking's application.

2. Feature

- Operation rage : 2.7V ~ 3.5V
- 50μm * 50μm CMOS active square pixel.
- Number of effective pixel 32 * 32.
- Total number of pixels 34 * 34.
- On-chip integrated video amplifier.
- No color filter.
- On-chip integrated AD converter.
- AD converter 2MHz with sampling rate and 6 bit resolution.
- External clock is 3.58MHz

3. Applications

- Motion detection
- Interactive toy
- Interactive TV Game
- Interactive PC Game

4. Pin configurations (package)

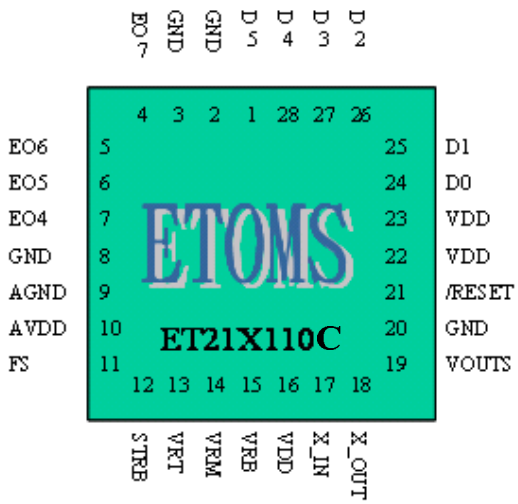


Fig.1. Pin assignment

5. Pin descriptions

Pin Name	Pin Type	Pin Description
Power		
VDD	Power	Power
GND	GND	Ground
AVDD	power	Analog power
AGND	GND	Analog ground
/RESET	I	Reset the sensor.
Sensor		
EO(7:4)	I	Set up exposure time. EO(3:0) = (1111)
/STR	O	Image data output trigger signal.(/STR is the signal that connect to ADSTART.)
FS	O	Frame output flag from sensor (FS is the signal that connect to ADCE.)
VoutS	O	Analog image data output (VoutS is the signal that connect to ADVIN.)
XTL-IN	I	Crystal oscillator Input
XTL-OUT	O	Crystal oscillator Output
AD		
D(5:0)	O	AD data output
VREFT	I	Voltage at top of reference resistor of AD converter. Connect a capacitor(1uF min.) to ground.
VREFM	I	Voltage at middle of reference resistor of AD converter. Connect a capacitor (1uF min.) to ground.
VREFB	I	Voltage at bottom of reference resistor of AD converter. Equal to the voltage of Vref (reference voltage for sensor). Connect a capacitor (1uF min.) to ground.

Note (1): FS: When CMOS start to output image data, this pin will pull high, otherwise pull low.

6. Functional block diagram

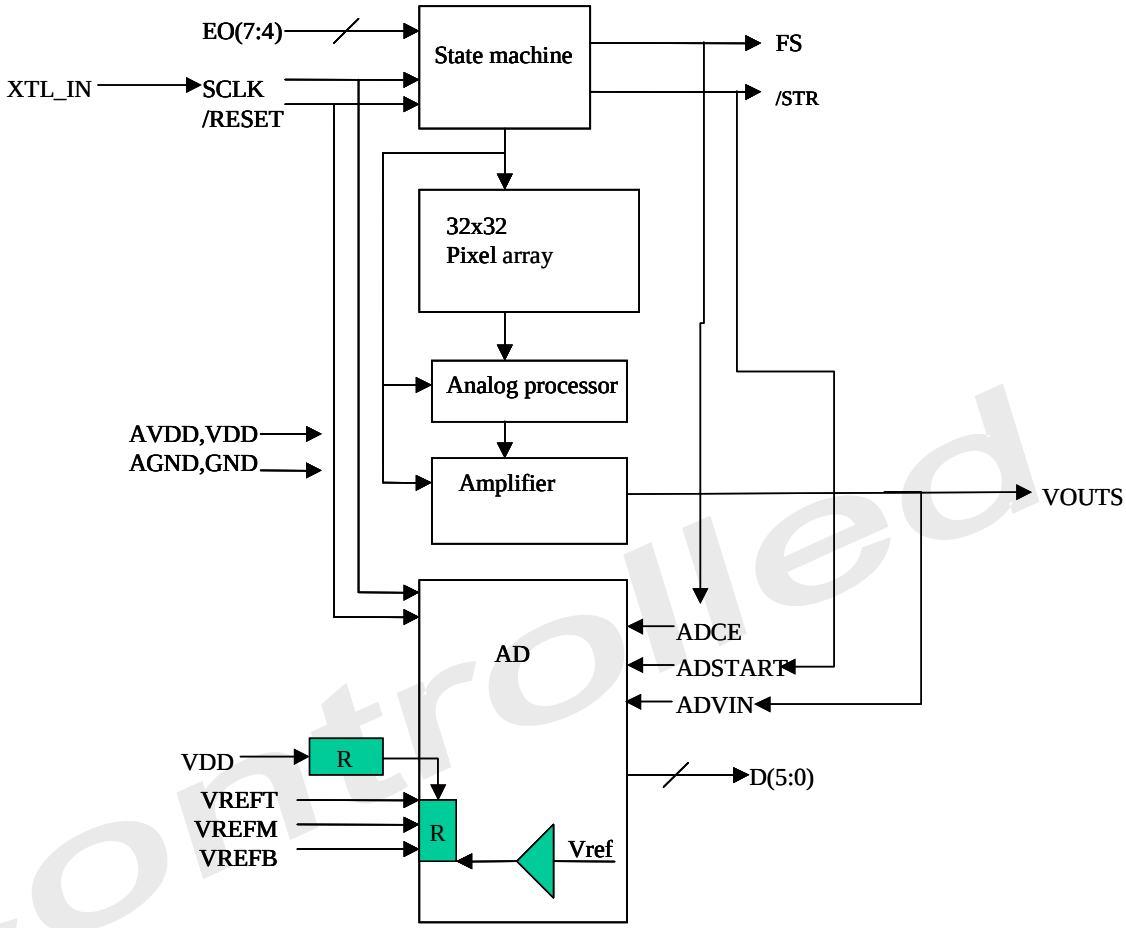


Fig.2. Block diagram

7. Function description

Exposure time control

EO7 to EO4 are the control signals for sensor exposure time. With internal EO3 to EO0 (default = EO(3:0)=(1111), They divide the exposure time (FS is low level) into 255 units. User can change EO7 to EO4 to fit user's exposure time. These IO can change when ever the sensor is running or not. But the new value will be used by next frame.

EO7:EO0	Exposure time	FS	Note
11111111	255 unit exposure time	0	
10001111	143 unit exposure time	0	
00011111	31 unit exposure time	0	
00001111	15 unit exposure time	0	

Sensor control timing

After power on, the sensor will load new IO setting (EO7 to EO4) and generate the timing as figure 3. FS is the frame signal for external circuit synchronous. It is a fixed timing. When FS is low level, the sensor is at exposure period. And when FS is high level, the sensor is at data transfer period.

The exposure period is depending on the EO7 to EO0 setting. The exposure time Texp divide into 255 parts. The sensor wills exposure as long as the time of EO (7:0) setting. For example, if the EO (7:0) is 16 and the exposure time will be Texp *16 /255.

At FS is high level; the data is ready for transferring. User can check STR signal, if there is a falling edge and user can get an analog signal (VOUTS). The VOUTR is the initial voltage (reset voltage) of sample and hold circuit before sampling a pixel data. The STR signal can be the start signal for AD converter circuit.

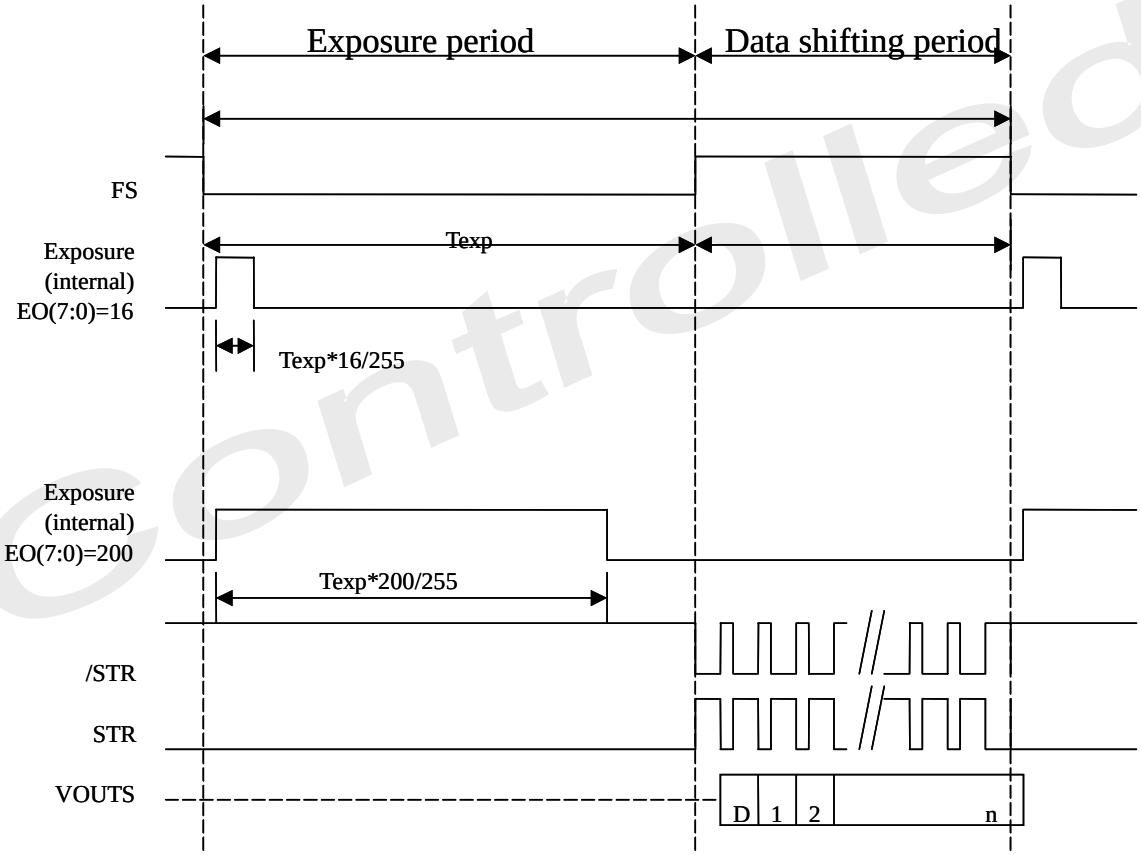


Fig.3. Sensor timing

Sensor data transfer

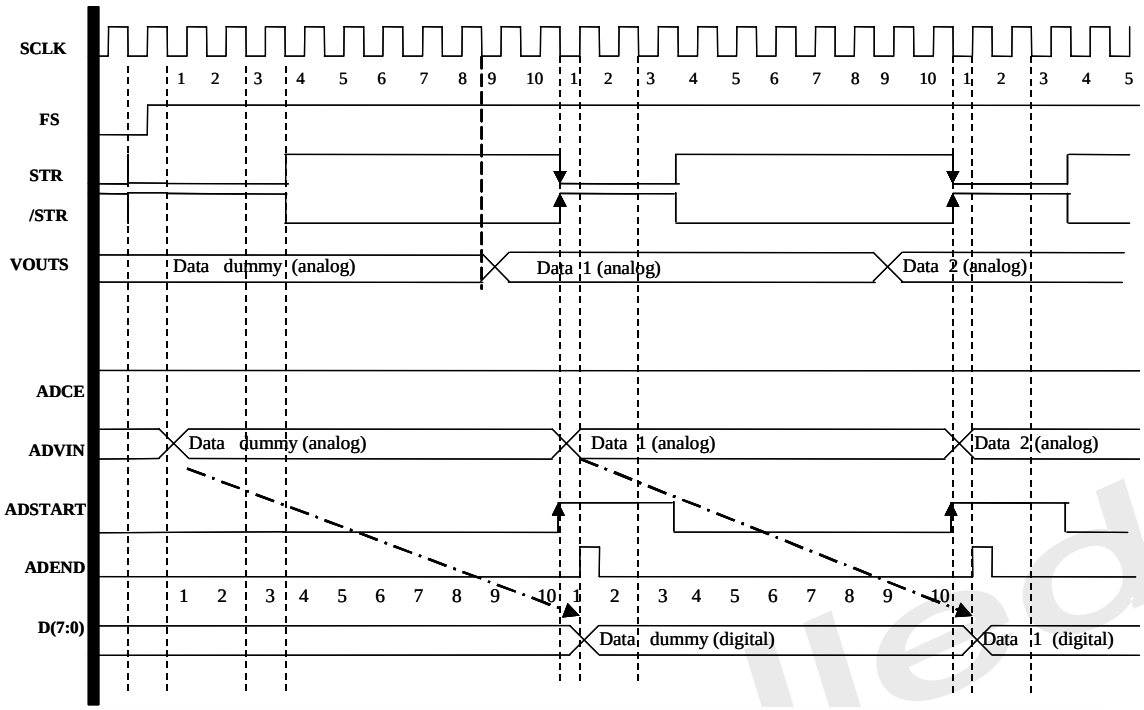
Figure 4 is the sensor array diagram. There is a guard ring of dummy sensor (D) outside the internal sensor (P).
The sensor is setting as 32 by 32 sensor. The flow of data transfer is (ROW, COLUMN)
A dummy STR => (0,0) =>(0,1) => (0,2)=>…….=>(0,30) => (0,31) =>
A dummy STR => (1,0) =>(1,1) => (1,2)=>…….=>(1,30) => (1,31) =>
…….=>
A dummy STR => (31,0) =>(31,1) => (31,2)=>…….=>(31,30) => (31,31) => stop

	column	0	1	2	3	….	30	31	32
ROW	D	D	D	D	D	….	D	D	D
0	D	P	P	P	P	….	P	P	D
1	D	P	P	P	P	….	P	P	D
2	D	P	P	P	P	….	P	P	D
3	D	P	P	P	P	….	P	P	D
:	D	P	P	P	P	….	P	P	D
30	D	P	P	P	P	….	P	P	D
31	D	P	P	P	P	….	P	P	D
32	D	D	D	D	D	….	D	D	D

Fig.4. Sensor array diagram

The relationship between SCLK and /STR

A STR is low pulse imply a new data ready on the VOUTS pin. Please refer to Figure 5.



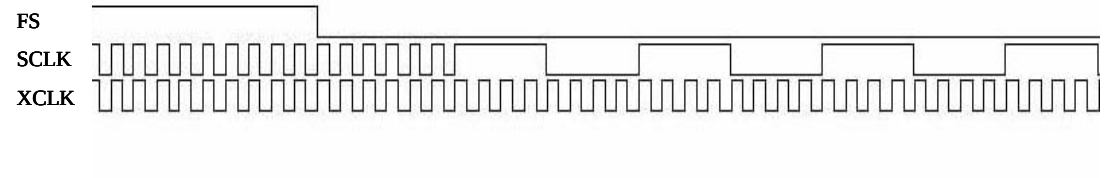


Fig.5. STR timing diagram for 32x32

Spectral Response

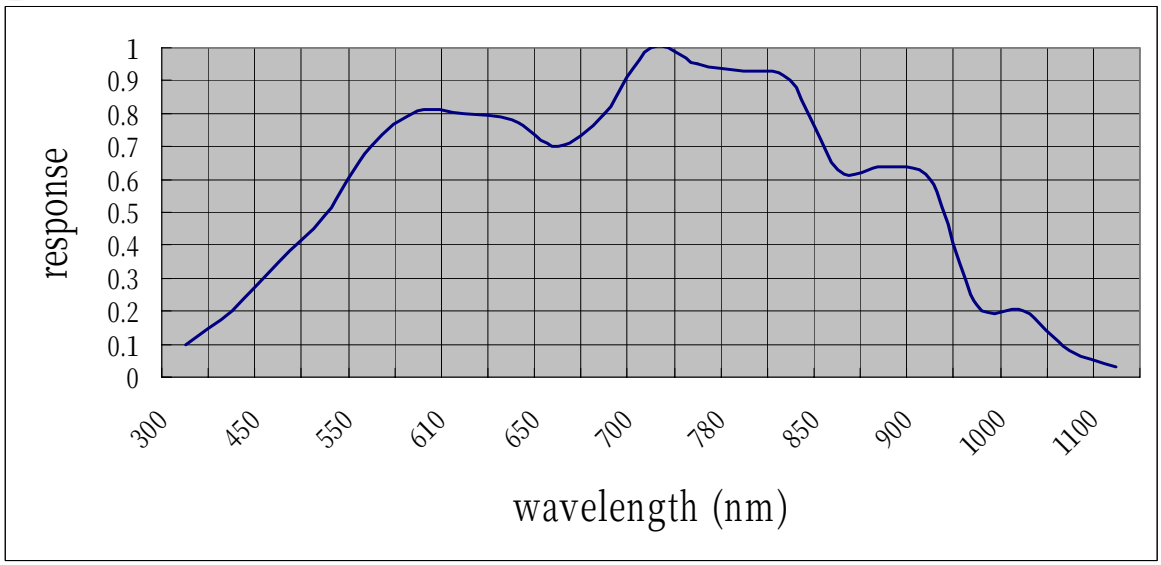


Fig.6. Spectral response

AD converter

The AD converter can use with internal sensor or by itself independently. ADCE (FS) is an enable signal. Set to high level, it will waiting ADSTART (/STR) signal for the sampling.

The AD needs ten XCLK for a sampling after a start ADSTART signal. It will generate an ADEND signal for external circuit interrupt for data accessing. Once the ADEND generated, the data will be ready on data bus D (5:0) and waiting for the next ADSTART signal.

The circuit can operate up to 20 MHZ clock (2MHz sampling rate) with 6-bit resolution.

If user want to get sensor digital signal, user can connect these pins. The /STR pin connect to ADSTART pin. The analog signal VOUT connects to ADVIN pin. After a rising edge of /STR (ADSTART), AD circuit will sample VOUTS (ADVIN) at next rising edge of XCLK. A sample needs ten XCLK, then latches digital data at D (5:0) and generates an ADEND signal for interruption. At the same time, next STR (ADSTRAT) comes and starts AD to sample next VOUTS (ADVIN).

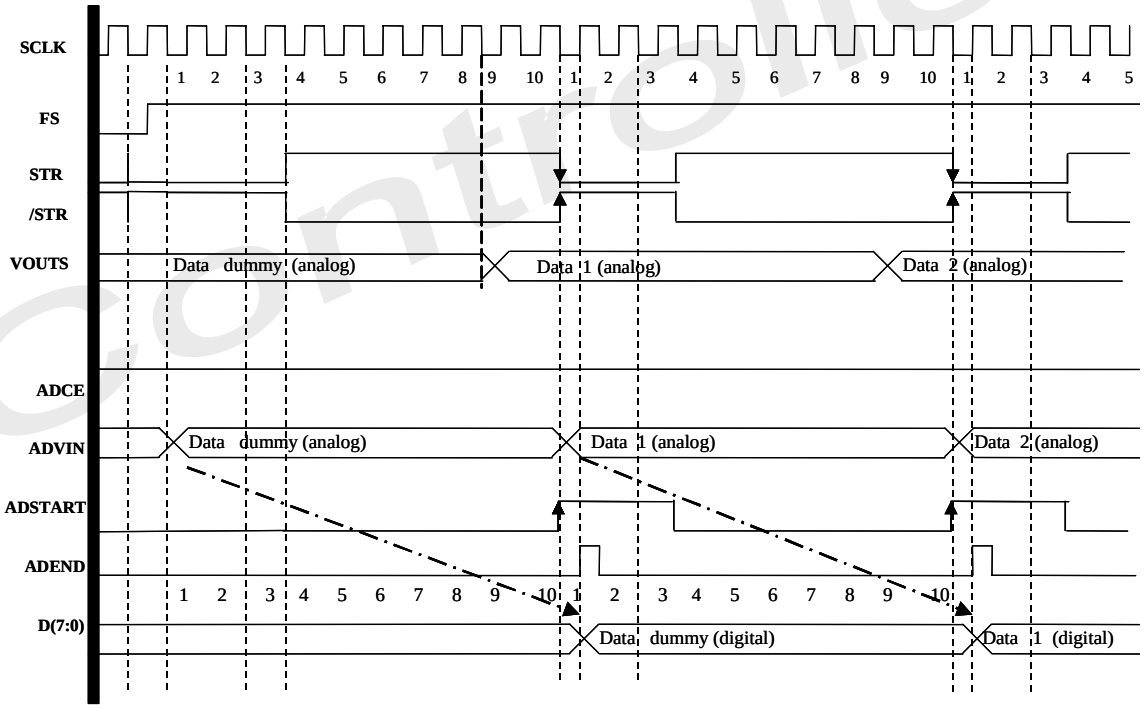


Fig.7. AD control timing

8. Absolute maximum rating

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD		-0.3 to VDD+0.3	V
Input voltage	VIN		-0.5 to VDD +0.5	V
Operating temperature range	TOPR		0 to +45	^{o}C
Storage temperature range	TSTR		-25 to +100	^{o}C

9. DC electrical characteristics

9.1 Operating condition, DC &AC Characteristics (condition : Ta= 0~+45 ^{o}C, VDD= 3.3 +/- 0.3V)

Characteristic	Symbol	Condition	Min.	Typical	Max.	Unit
Power supply	VCC	-	2.7	3.3	3.6	V
"H" logic input voltage	VIH	-	0.7*VDD	--	VDD	V
"L" logic input voltage	VIL		0	--	0.3*VDD	V
"H" digital output voltage	VOH	IOH = -1.5mA for digital IO (FS, STR)	2.4	--	VDD	V
"L" digital output voltage	VOL	IOL = 2.0mA for digital IO (FS, STR)	0	--	0.4	V
Input threshold voltage (Schmitt) for SCLK pin	VT+ VT-	-	0.5*VDD 0.2*VDD	--	0.75*VDD 0.4*VDD	V
Input leakage current	IIL	Vin=VDD, GND	-	-	+/-1	μA
Bandwidth of the on-chip video Amplifier	--		--	40	--	MHz
Digital power current consumption	--	EO(7:0)=0 SCLK=3.58MHz	--	4	6	mA
Analog power current consumption (AD + sensor)	--	EO(7:0)=0 SCLK=3.58MHz	--	5	6	mA

9.2 sensor Characteristics

Characteristic.	Value	Description

Pixel Size	50um* 50um	Square pixel
Sensitivity	30000V/(W.sec/M*M)	Primary video O/P without amplification.
Spectrum Span	400-1100nm	
Saturation Signal Amplitude	>0.8V	Measured at primary video O/P at 25 degree C.
Fixed Pattern Noise	15mV	Measured at primary video O/P at 25 degree C.
Random Noise	<2mV	Measured at primary video O/P at 25 degree C.
Dark Current in Photo-sensor	<2V/s	Measured at primary video O/P at 25 degree C.
Analog output external load (VOUTS)	1 KΩ // 2pF	The 1K resistor connects to external component by series connecting. The 2pF is connecting from resistor to ground.
Output voltage at dark.	1.6V	VOUTS,VOUTR
Output voltage at saturation	3.0V	VOUTS

9.3 Operating condition, AD Characteristics
(Condition: Ta= 0~+45 °C, VDD= 2.9 +/- 0.3V)

Characteristic	Symbol	Min.	Typical	Max.	Unit
Sampling rate	Fsamp			2	MHz
AD internal reference voltage	Vref	1.2	1.5	1.8	V
Differential nonlinear error	DNL			**±1/2**	LSB
Integral nonlinear error	INL			**±1**	LSB
Conversion time	**Tcv**			**0.5**	**uS**
Voltage at the top of reference resistor.	**VRT**		(VDD-Vref)/2+Vref		**V**
Voltage at the middle of reference resistor.	**VRM**		(VDD-Vref)/4+Vref		**V**
Voltage at the bottom of reference resistor.	**VRB**		Vref		**V**

10. AC electrical characteristics

Characteristic	Symbol	Min.	Typical	Max.	Unit
System Frequency	SCLK	0.5	3.58	12	MHz
Data setup time	Tsetup	50	100		nS
Data hold time	Thold	50	100		nS

11. Timing diagrams

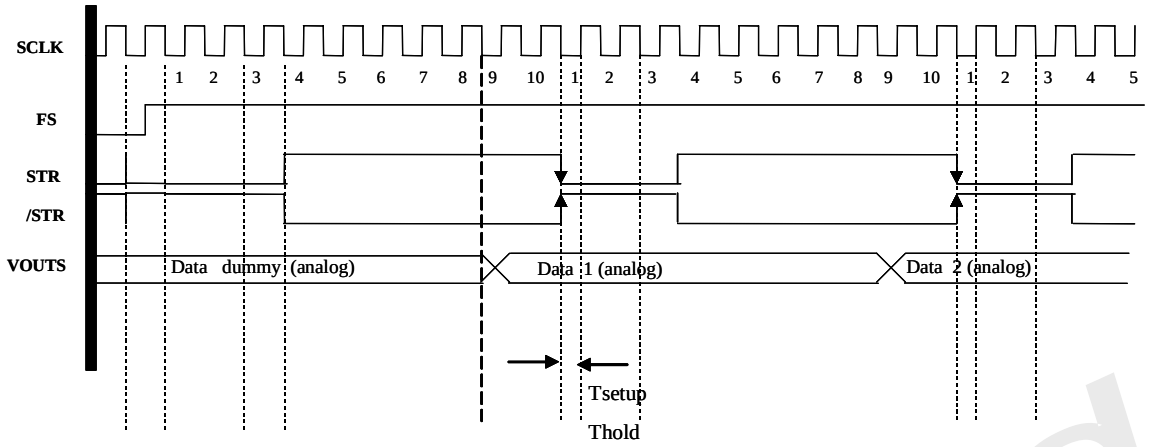


Fig.8. AC timing

12. Application circuit

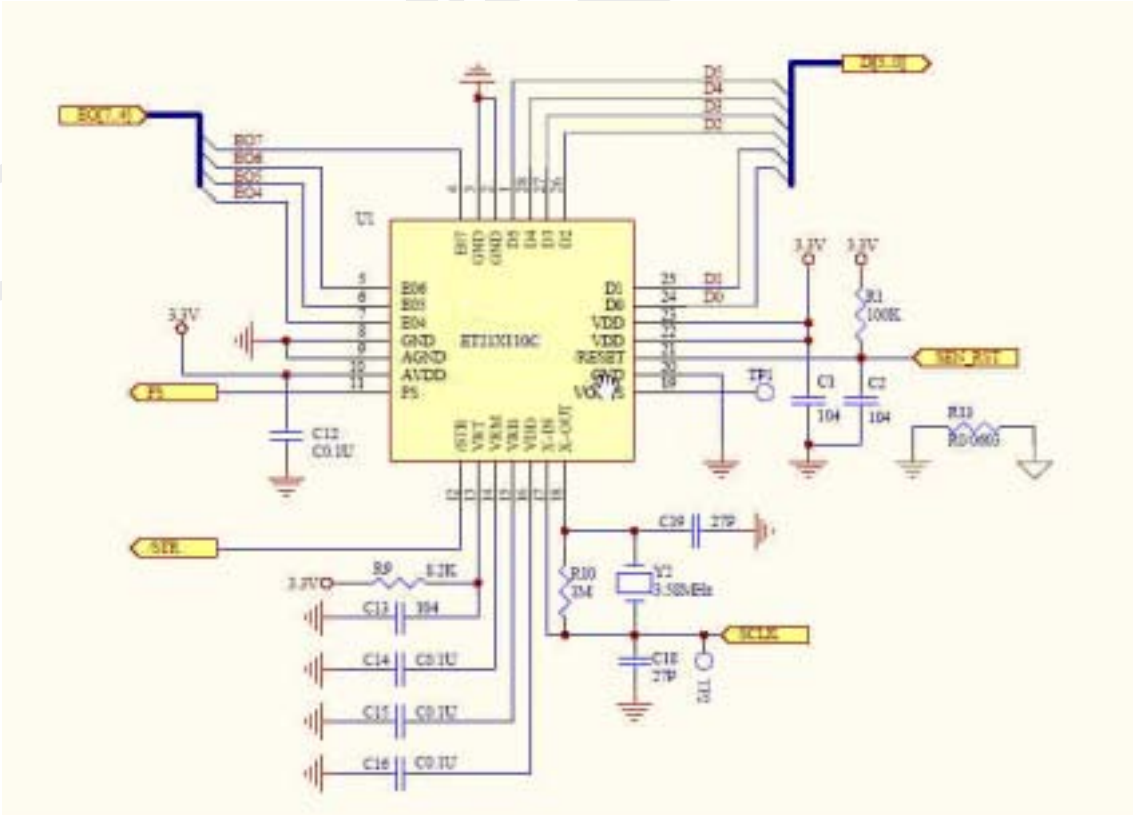


Fig. 9. Application circuit

13. History

Version	Date	Description
V1	2005/09/13	New Creation
V2	2006/08/09	Delete P.6 of package description. Add appendix – package type table.
V3	2007/04/09	1. Add more application field of Chapter 3 (P.1). 2. Modify the pixel size information to 50umx50um (P.1; P.9).

Appendix

A. Package Type

Product No.	Package Type	Pin Count	Package Size
ET21X110CN	BQFN	28	11.43mmx11.43mm