CIRRUS EDB9301 ENGINEERING DEVELOPMENT BOARD

REVISION2

SHEET 1 OF 6

Audio
PG5_Audio.sch

CS9301
PG2_CS9301.sch

Power1
PG6_Power1.sch

Ethernet1
PG4_Ethernet1.sch

9301 memory schematic
PG3_9301_Memory.SCH

Notes: (unless otherwise stated)

1. All resistors are listed in ohms and are 5%, 1/10 W, Metal Film (0603 form factor)
2. All capacitors are listed in microfarads, and are 10%, 25V, Ceramic, X7R (0603 form factor)
3. All inductors are listed in microhenries, and are 5%, 100ma, non-wound (0805 form factor)
4. Signal Ports are global, and are all connected through sheet symbols
5. Signal Names are local, and apply only to the current sheet.

Sheet Index

ECN CHANGES FROM REV 1 TO REV 2

1. Change C53 to 47pf
2. Reverse power and ground on U8
3. Make sure all jumpers are correctly called out on the schematics the way they are to be connected on the board.
4. Remove signal SDOUT from JP12 and put signal SDIN in place.
5. Remove USB Maxim power switch and add fuse in place.
6. Correct alignment with GPIO headers.
7. Remove legend and put silkscreen at jumper location
8. Move headers for test0 and test1 over to allow for easier access. Also have test0 to outside edge of board
9. remove bottom silkscreen
10. Add correct silk for RS232 com ports for Uart1 and Uart2
11. change LED2 to red
12. place DNP 1x2 header for alternative power source.
13. On pin 14 of audio dac remove net resetn and place egpio1 net in place. Place a 1K pull down on the egpio1 line.

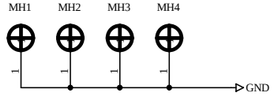
LOGO1

CIRRUS_LOGO

GLOBAL FIDUCIALS

TOP SIDE

FL4 FL5 FL6



Title		*Videon Central Inc* *2171 Sandy Drive* *Second Floor* *State College , PA 16803*
Size: B	Revision: 2	
Sheet 1 of 6		Date: 22-Jan-2004

CIRRUS 9301 SCHEMATIC

SHEET 2 OF 6

REVISION 2

DECOUPLING ON POWER PAGE

RS232 INTERFACE

NEED TO CONFIRM ADDRESS PINS

Multi-ICE Connector

DEFAULT NOT INSTALLED

SET TO 2:3 FOR NORMAL OPERATION
SET TO 1:2 FOR DOWNLOAD

USB INTERFACE

BOTTOM CONNECTOR

TOP CONNECTOR

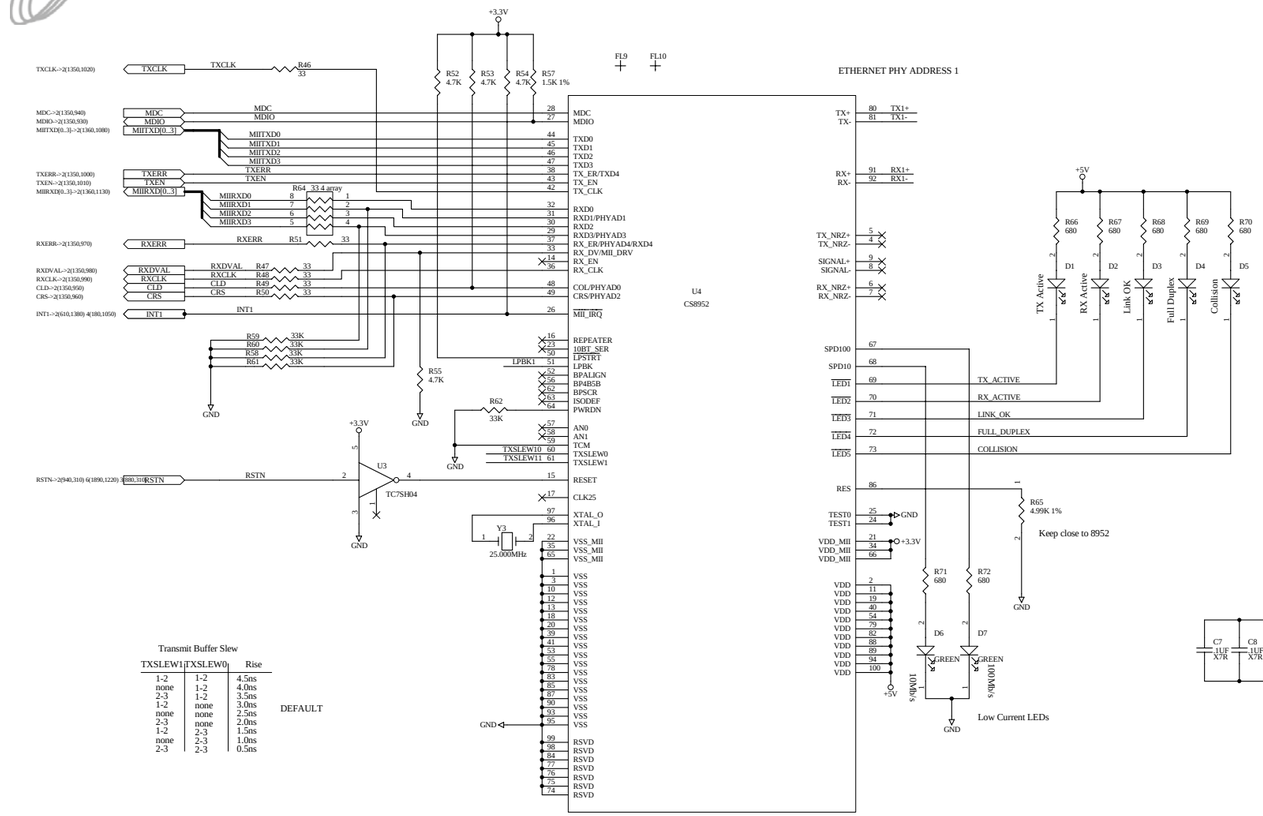
DUAL PORT "STACKED" DSUB CONNECTORS

Title		
Size: C	Number	Revision
Date: 22-Jan-2004	Sheet of	
File:		

ETHERNET INTERFACE (MII Address) SCHEMATIC

SHEET 4 OF 6

REVISION 2

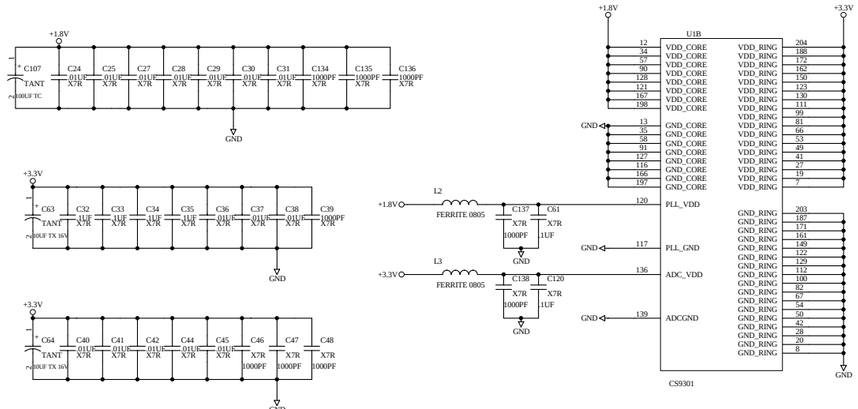


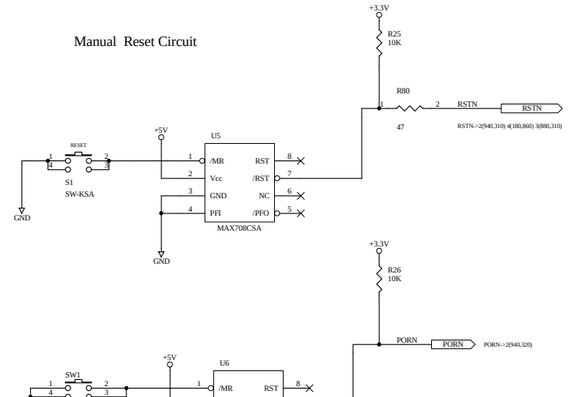
Title		
ETHERNET INTERFACE SCHEMATIC		*Videon Central Inc* *2171 Sandy Drive* *Second Floor* *State College, PA 16803*
Size: B	Revision: 2	
Sheet 4 of 6		Date: 22-Jan-2004

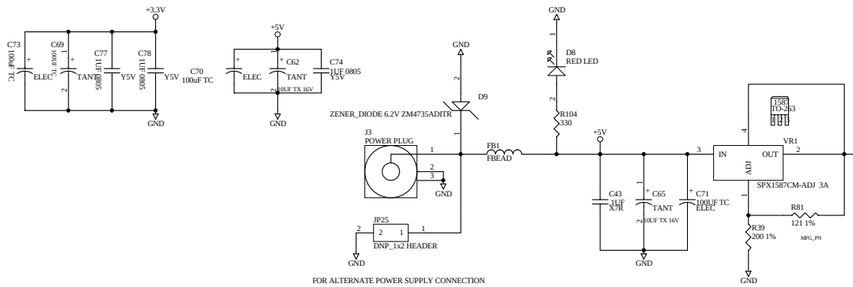
POWER SCHEMATIC

SHEET 6 OF 6

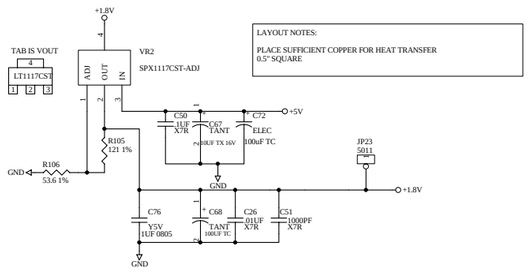
REVISION 2



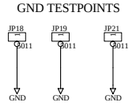




+1.8V REGULATION



GND TESTPOINTS

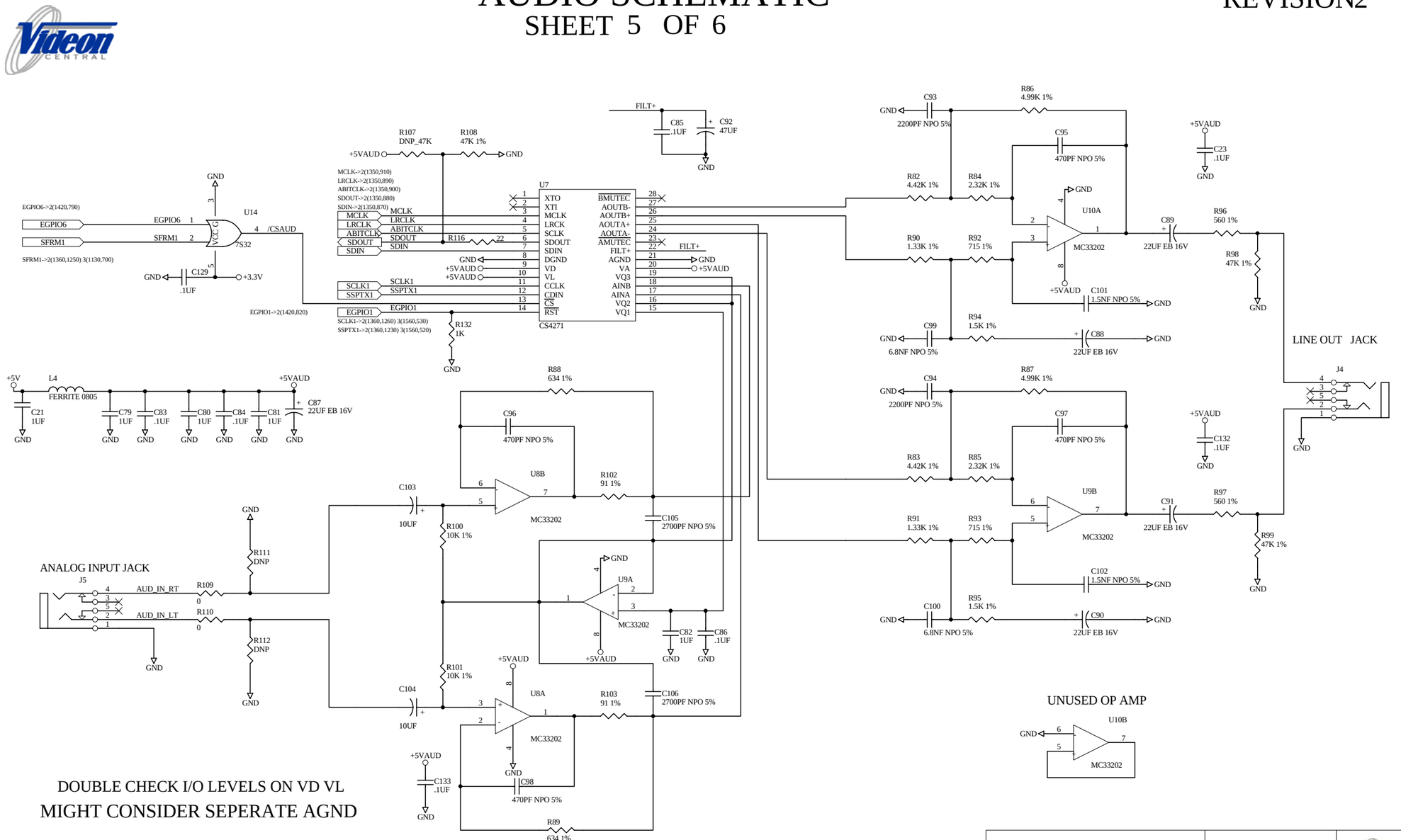


Title: **POWER SCHEMATIC**		Videon Central Inc 2171 Sandy Drive Second Floor State College, PA 16803	
Size: B	Revision: 2		
Sheet 6 of 6		Date: 22-Jan-2004	

AUDIO SCHEMATIC

SHEET 5 OF 6

REVISION2



Title	
Size: B	Revision: 2
Sheet 5 of 6	

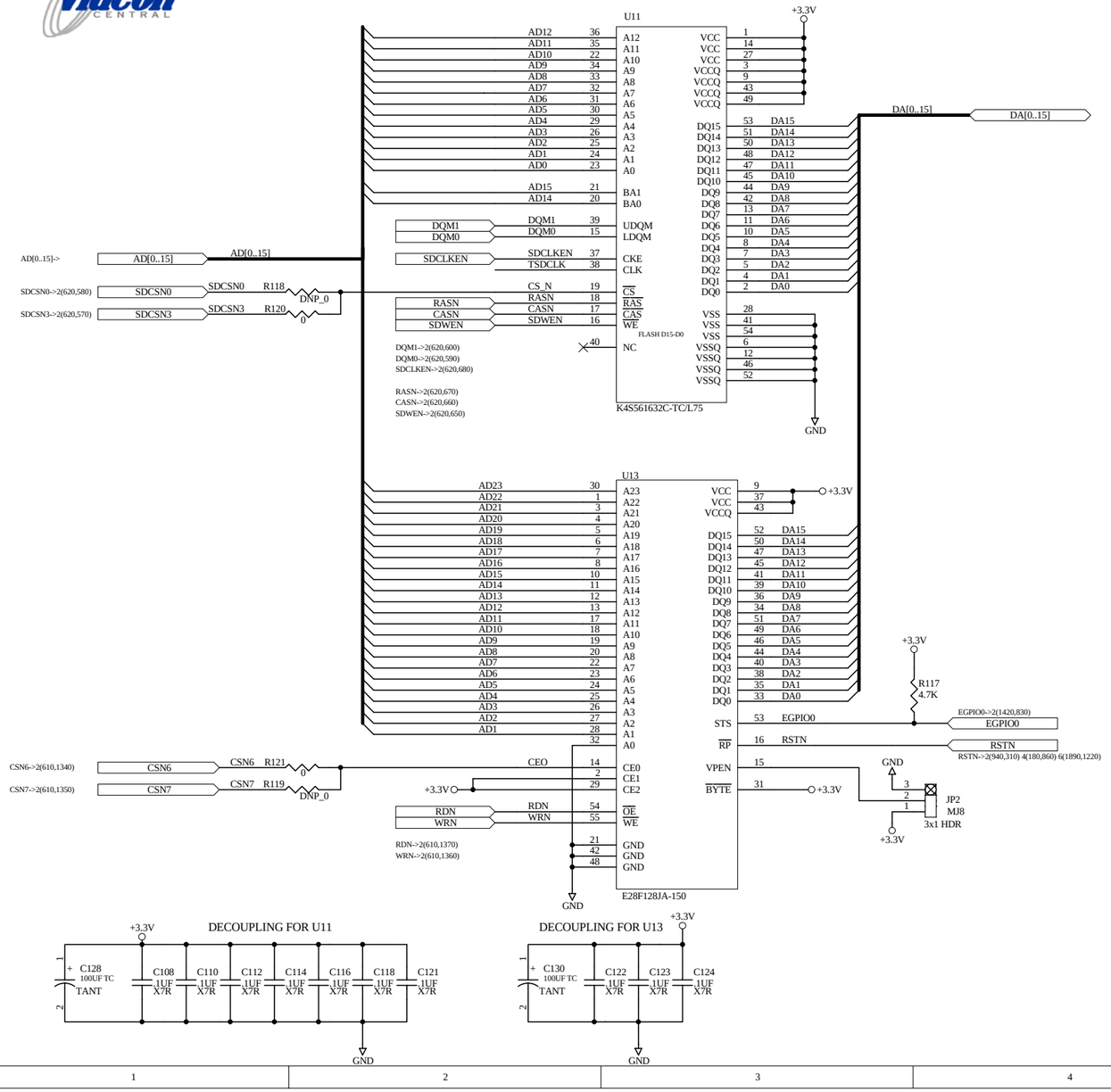
Videon Central Inc
2171 Sandy Drive
Second Floor
State College , PA 16803

Date: 22-Jan-2004

9301 MEMORY & FLASH SCHEMATIC

SHEET 3 OF 6

REVISION2



EEPROM INTERFACE

Title		*Videon Central Inc* *2171 Sandy Drive* *Second Floor* *State College , PA 16803*	
Size: B	Revision: 2		
Sheet 3 of 6		Date: 22-Jan-2004	