Chapter 4

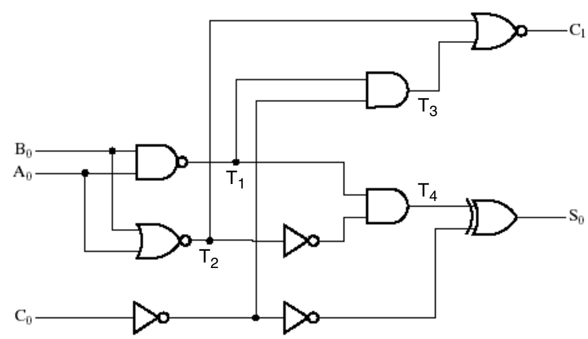
4-2.*

$$C_1 = \overline{T_3 + T_2} = \overline{T_1\bar{C}_0 + T_2} = \overline{\overline{A_0B_0}\,\overline{C_0} + \overline{A_0 + B_0}} = \overline{(\bar{A}_0 + \bar{B}_0)\bar{C}_0 + \bar{A}_0\bar{B}_0} = (A_0B_0 + C_0)(A_0 + B_0)$$

$$C_1 = A_0B_0 + A_0C_0 + B_0C_0$$

$$S_0 = C_0 \oplus T_4 = C_0 \oplus T_1\bar{T}_2 = C_0 \oplus \overline{A_0B_0}(A_0 + B_0) = C_0 \oplus (\bar{A}_0 + \bar{B}_0)(A_0 + B_0) = C_0 \oplus A_0\bar{B}_0 + \bar{A}_0B_0$$

$$S_0 = A_0 \oplus B_0 \oplus C_0$$



4-3.*

Unsigned	1001 1100	1001 1101	1010 1000	0000 0000	1000 0000
1's Complement	0110 0011	0110 0010	0101 0111	1111 1111	0111 1111
2's Complement	0110 0100	0110 0011	0101 1000	0000 0000	1000 0000

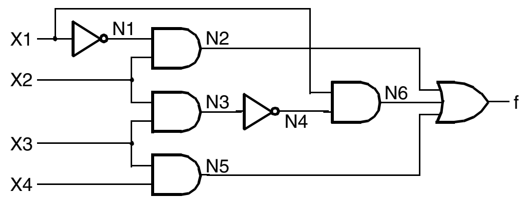
4-6.*

+36	=	0100100	36		0100100
- 24	=	1101000	+(–24)	+	1101000
- 35	=	1011101			10001100
			= 12	=	0001100
			–35		1011101
			- (–24)	+	0011000
			= –11	=	1110101

4-16.*

	S	A	B	C_4	S_3	S_2	S_1	S_0
a)	0	0111	0111	0	1	1	1	0
b)	1	0100	0111	0	1	1	0	1
c)	1	1101	1010	1	0	0	1	1
d)	0	0111	1010	1	0	0	0	1
e)	1	0001	1000	0	1	0	0	1

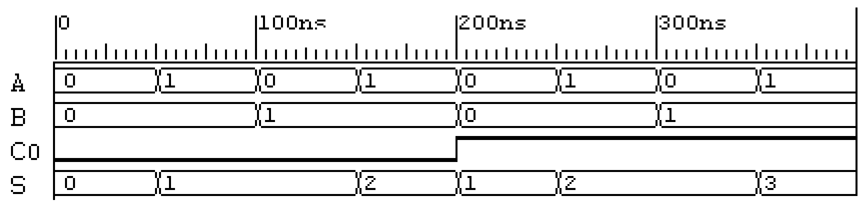
4-20.*

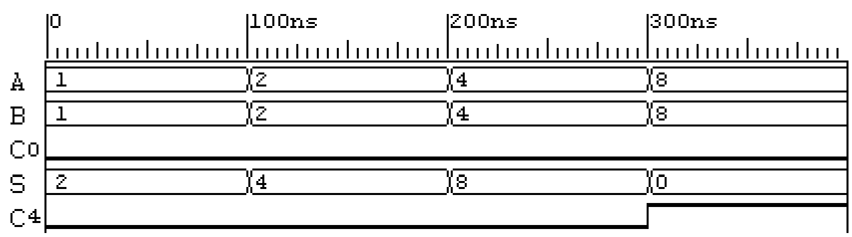


4-24.*

```
begin
    F <= (X and Z) or ((not Y) and Z);
end;
```

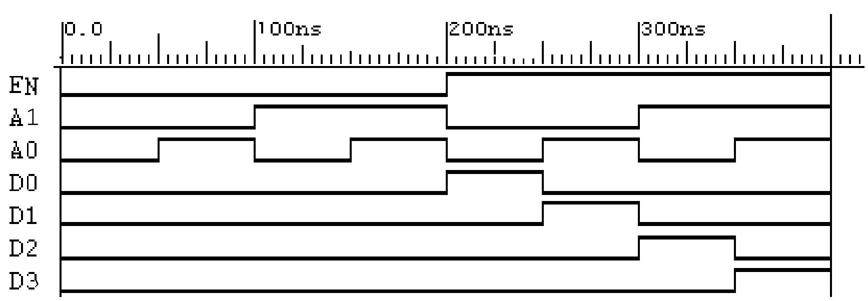
4-29.*



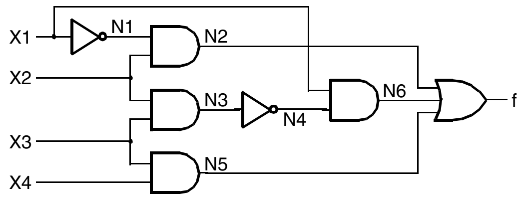


The solution given is very thorough since it checks each of the carry connections between adjacent cells transferring 0 and 1. In contrast a test applying C0 = 1 and A = 15 with B = 0 would allow a whole variety of incorrect connections between cells that would not be detected.

4-31.*(Errata: Replace "E" with "EN".)



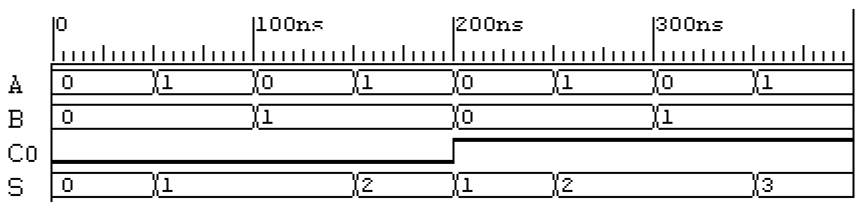
4-34.*

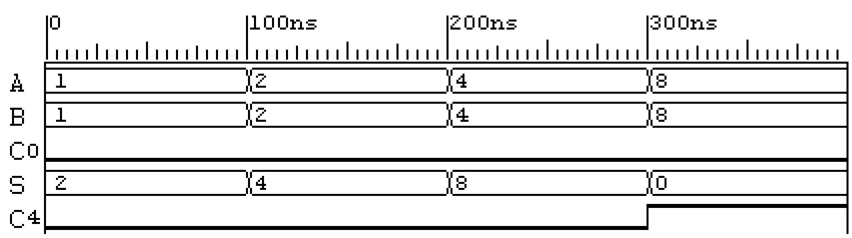


4-38.*

```
module circuit_4_53(X, Y, Z, F);
  input X, Y, Z;
  output F;
  assign F = (X & Z) | (Z & ~Y);
endmodule
```

4-43.*





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