**Solutions to Problems Marked with a * in**
**Logic and Computer Design Fundamentals, 4th Edition**

# Chapter 6



## 6-1.*

a) $F = (\overline{A} + B)\ C\ D$

b) $G = (A + \overline{B})\ (\overline{C} + D)$

## 6-4*

The longest path is from input C or $\overline{D}$.

0.073 ns + 0.073 ns + 0.048 ns + 0.073 ns = 0.267 ns

## 6-10.*

a) The longest direct path delay is from input X through the two XOR gates to the output Y.

$$t_{delay} = t_{pdXOR} + t_{pdXOR} = 0.20 + 0.20 = 0.40 \text{ ns}$$

b) The longest path from an external input to a positive clock edge is from input X through the XOR gate and the inverter to the B Flip-flop.

$$t_{delay} = t_{pdXOR} + t_{pd\ INV} + t_{sFF} = 0.20 + 0.05 + 0.1 = 0.35 \text{ ns}$$

c) The longest path delay from the positive clock edge is from Flip-flop A through the two XOR gates to the output Y.

$t_{delay} = t_{pdFF} + 2\ t_{pdXOR} = 0.40 + 2(0.20) = 0.80$ ns

d) The longest path delay from positive clock edge to positive clock edge is from clock on Flip-flop A through the XOR gate and inverter to clock on Flip-flop B.

$$t_{delay\text{-clock edge to clock edge}} = t_{pdFF} + t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.40 + 0.20 + 0.05 + 0.10 = 0.75 \text{ ns}$$

e) The maximum frequency is $1/t_{delay\text{- clock edge to clock edge}}$. For this circuit, $t_{delay\text{-clock edge to clock edge}}$ is 0.75 ns, so the maximum frequency is 1/0.75 ns = 1.33 GHz.

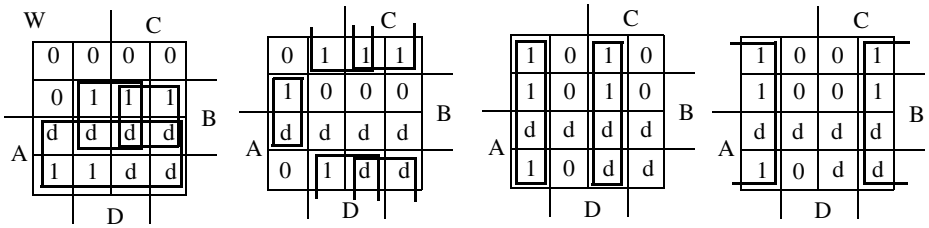
Comment: The clock frequency may need to be lower due to other delay paths that pass outside of the circuit into its environment. Calculation of this frequency cannot be performed in this case since data for paths through the environment is not provided.

**6-13.*** (Errata: Change "32 X 8" to "64 X 8" ROM)

| IN | OUT | IN | OUT | IN | OUT | IN | OUT |
|---|---|---|---|---|---|---|---|
| 000000 | 0000 0000 | 010000 | 0001 0110 | 100000 | 0011 0010 | 110000 | 0100 1000 |
| 000001 | 0000 0001 | 010001 | 0001 0111 | 100001 | 0011 0011 | 110001 | 0100 1001 |
| 000010 | 0000 0010 | 010010 | 0001 1000 | 100010 | 0011 0100 | 110010 | 0101 0000 |
| 000011 | 0000 0011 | 010011 | 0001 1001 | 100011 | 0011 0101 | 110011 | 0101 0001 |
| 000100 | 0000 0100 | 010100 | 0010 0000 | 100100 | 0011 0110 | 110100 | 0101 0010 |
| 000101 | 0000 0101 | 010101 | 0010 0001 | 100101 | 0011 0111 | 110101 | 0101 0011 |
| 000110 | 0000 0110 | 010110 | 0010 0010 | 100110 | 0011 1000 | 110110 | 0101 0100 |
| 000111 | 0000 0111 | 010111 | 0010 0011 | 100111 | 0011 1001 | 110111 | 0101 0101 |
| 001000 | 0000 1000 | 011000 | 0010 0100 | 101000 | 0100 0000 | 111000 | 0101 0110 |
| 001001 | 0000 1001 | 011001 | 0010 0101 | 101001 | 0100 0001 | 111001 | 0101 0111 |
| 001010 | 0001 0000 | 011010 | 0010 0110 | 101010 | 0100 0010 | 111010 | 0101 1000 |
| 001011 | 0001 0001 | 011011 | 0010 0111 | 101011 | 0100 0011 | 111011 | 0101 1001 |
| 001100 | 0001 0010 | 011100 | 0010 1000 | 101100 | 0100 0100 | 111100 | 0110 0000 |
| 001101 | 0001 0011 | 011101 | 0010 1001 | 101101 | 0100 0101 | 111101 | 0110 0001 |
| 001110 | 0001 0100 | 011110 | 0011 0000 | 101110 | 0100 0110 | 111110 | 0110 0010 |
| 001111 | 0001 0101 | 011111 | 0011 0001 | 101111 | 0100 0111 | 111111 | 0110 0011 |

**6-19.***

Assume 3-input OR gates.




$W = A + BC + BD$ $X = B\overline{C}\,\overline{D} + \overline{B}C + \overline{B}D$ $Y = CD + \overline{C}\,\overline{D}$ $Z = \overline{D}$

Each of the equations above is implemented using one 3-input OR gate. Four gates are used.