Logic and Computer Design Fundamentals

Chapter 6 – Selected Design Topics

Part 1 – The Design Space

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(Hyperlinks are active in View Show mode)

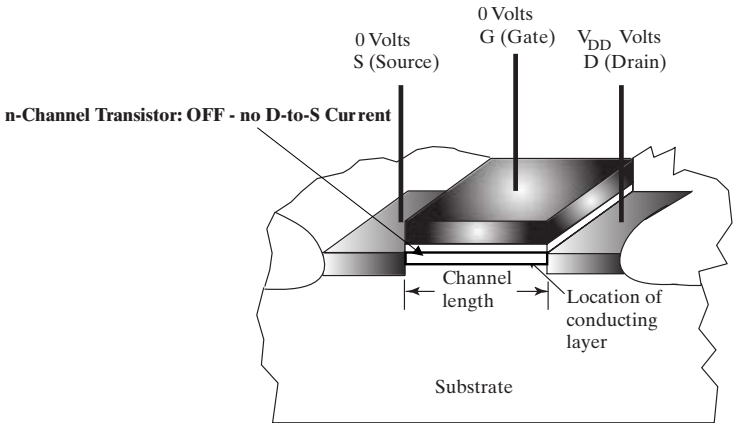
Overview

- **Part 1 – The Design Space**
  - **Integrated Circuits**
    - **Levels of Integration**
  - **CMOS Circuit Technology**
    - **CMOS Transistor Models**
    - **Circuits of Switches**
    - **Fully Complementary CMOS Circuits**
    - **Technology Parameters**
- **Part 2 – Propagation Delay and Timing**
- **Part 3 – Asynchronous Interactions**
- **Part 4 - Programmable Implementation Technologies**

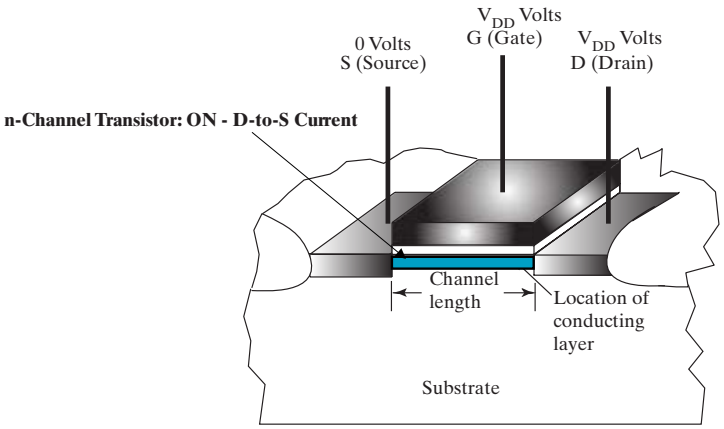
Integrated Circuits

- **Integrated circuit (informally, a "chip") is a semiconductor crystal (most often silicon) containing the electronic components for the digital gates and storage elements which are interconnected on the chip.**
- **Terminology - Levels of chip integration**
  - ***SSI* (*small-scale integrated*) - fewer than 10 gates**
  - ***MSI* (*medium-scale integrated*) - 10 to 100 gates**
  - ***LSI* (*large-scale integrated*) - 100 to thousands of gates**
  - ***VLSI* (*very large-scale integrated*) - thousands to 100s of millions of gates**

MOS Transistor

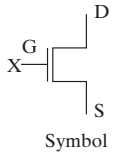


MOS Transistor



Switch Models for MOS Transistors

- **n-Channel – Normally Open (NO) Switch Contact**

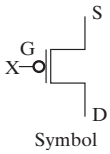


Symbol

Switch Model:

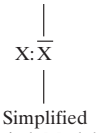
Simplifed
Switch Model

- **p-Channel – Normally Closed (NC) Switch Contact**



Symbol

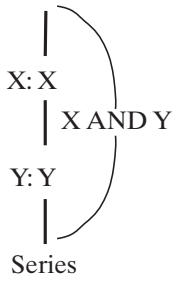
Switch Model



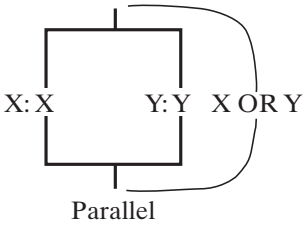
Simplified
Switch Model

Circuits of Switch Models

- **Series**

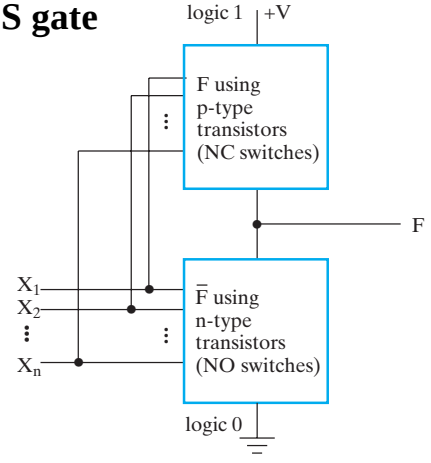


- **Parallel**



Fully-Complementary CMOS Circuit

- **Circuit structure for fully-complementary CMOS gate**



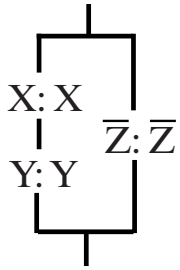
General Structure

CMOS Circuit Design Example

- **Find a CMOS gate with the following function:** $F = \overline{X}\,Z + \overline{Y}\,Z = (\overline{X} + \overline{Y})Z$
- **Beginning with F0, and using $\overline{F}$**

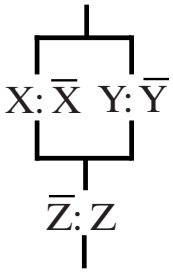
$$\text{F0 Circuit: } \overline{F} = X\,Y + \overline{Z}$$

- **The switch model circuit in terms of NO switches:**



CMOS Circuit Design Example

- **The switch model circuit for F1 in terms of NC contacts is the dual of the switch model circuit for F0:**



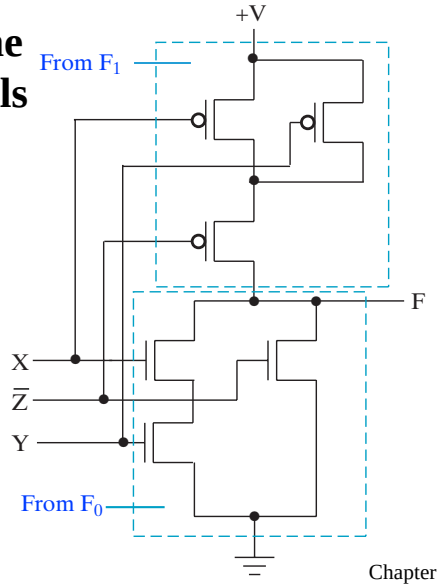
- **The function for this circuit is:**

$$\text{F1 Circuit: } F = (\overline{X} + \overline{Y})\,Z$$

which is the correct F.

CMOS Circuit Design Example

- **Replacing the switch models with CMOS transistors; note input $\overline{Z}$ must be used.**



Technology Parameters

- **Specific gate implementation technologies are characterized by the following parameters:**
  - ***Fan-in*** **– the number of inputs available on a gate**
  - ***Fan-out*** **– the number of standard loads driven by a gate output**
  - ***Logic Levels*** **– the signal value ranges for 1 and 0 on the inputs and 1 and 0 on the outputs (see Figure 1-1)**
  - ***Noise Margin*** **– the maximum external noise voltage superimposed on a normal input value that will not cause an undesirable change in the circuit output**
  - ***Cost for a gate*** **- a measure of the contribution by the gate to the cost of the integrated circuit**
  - ***Propagation Delay*** **– The time required for a change in the value of a signal to propagate from an input to an output**
  - ***Power Dissipation*** **– the amount of power drawn from the power supply and consumed by the gate**

Fan-out

- **Fan-out can be defined in terms of a standard load**
  - **Example: 1 standard load equals the load contributed by the input of 1 inverter.**
  - ***Transition time* -the time required for the gate output to change from H to L, t_{HL}, or from L to H, t_{LH}**
  - **The *maximum fan-out* that can be driven by a gate is the number of standard loads the gate can drive without exceeding its specified *maximum transition time***

Cost

- **In an integrated circuit:**
  - **The cost of a gate is proportional to the chip area occupied by the gate**
  - **The gate area is roughly proportional to the number and size of the transistors and the amount of wiring connecting them**
  - **Ignoring the wiring area, the gate area is roughly proportional to the gate input count**
  - **So gate input count is a rough measure of gate cost**
- **If the actual chip layout area occupied by the gate is known, it is a far more accurate measure**

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