Semiconductors

I²C Logic Selection Guide 2003

PHILIPS

I²C overview

Originally, the I²C bus was designed to interact within a small number of devices on a single card, such as to manage the tuning of a car radio or TV. The maximum allowable capacitance was set at 400 pF to allow proper rise and fall times for optimum clock and data signal integrity with a top speed of 100 kbit/s. In 1992, the maximum bus speed was increased to 400 kbit/s, to keep up with the ever-increasing performance requirements of new ICs. The latest I²C specification, released in 1998, increased top speed to 3.4 Mbit/s. All I²C devices are designed to be able to communicate together on the same two-wire bus and system functional architecture is limited only by the imagination of the designer.

While its application to bus lengths within the confines of consumer products such as PCs, cellular phones, car radios or TV sets grew quickly, only a few system integrators were using it to span long distances. The I²C bus is now being used in multiple card systems, such as a blade servers and rack mouted servers, where the I²C bus to each card needs to be easy to isolate to allow for card insertion and removal while the rest of the system is in operation. In some systems, many more devices may need to be located onto the same card, where before the total device and trace capacitance would have exceeded 400 pF. New bus extension & control devices help expand the I²C bus beyond the 400 pF limit of about 20 to 30 devices and help control more devices, even multiple identical devices with the same address. These new devices are popular with designers as they continue to expand and increase the use of the I²C bus in maintenance and control applications.

This selection guide focuses on general purpose devices like General Purpose I/O Expanders, LED Blinkers, Temperature and Voltage Hardware Monitors, DIP Switch Replacements, Multiplexers, Bus Masters/Microcontrollers, Bus Repeater/Hub/ Extenders, Serial EEPROMs, Voltage Level Translators and Analog to Digital Converters.

I²C features

- Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable through a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- I²C is a true multi-master bus including collision detection and arbitration, to prevent data corruption if two or more masters simultaneously initiate data transfers
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode
- On-chip filtering (50 ns) rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus segment is limited to a maximum bus capacitive loading of 400 pF

Semiconductors

I²C designer benefits

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic
- No need to design bus interfaces because the I²C-bus interface is already integrated on-chip
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time improves as designers quickly become familiar with the frequently used functional blocks represented by I²C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules

I²C manufacturers benefits

- The simple 2-wire serial I²C-bus minimizes interconnections so ICs have fewer pins and there are fewer PCB tracks; resulting in smaller and less expensive PCBs
- The completely integrated I²C-bus protocol eliminates the need for address decoders and other 'glue logic'
- The multi-master capability of the I²C-bus allows rapid testing/ alignment of end-user equipment via external connections to an assembly-line
- Increases system design flexibility by allowing simple construction of equipment variants and easy upgrading to keep design up-to-date
- The I²C-bus is a de facto world standard that is implemented in over 1000 different ICs (Philips has > 400) and licensed to more than 70 companies

Applications

There are some specific applications for certain types of I²C devices such as TV or radio tuners, but in most cases a general purpose I²C device can be used in many different applications because of its simple construction.

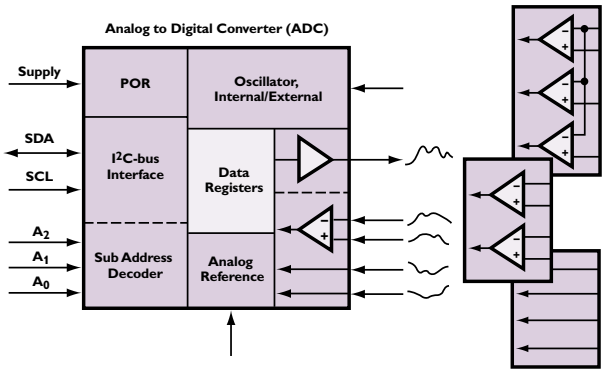
End use segment

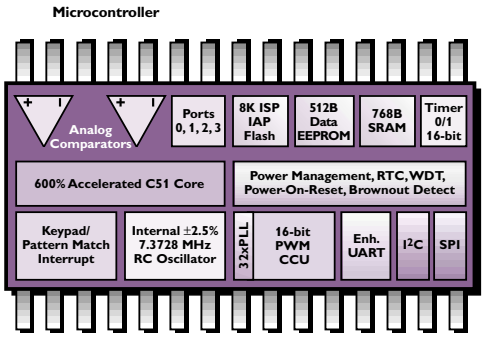
Telecom: Mobile phones, Base stations, Switching, Routers
Data processing: Laptop, Desktop, Workstation, Server
Instrumentation: Portable instrumentation, Metering systems
Automotive: Dashboard, Infotainment
Consumer: Audio/video systems, Consumer electronics (DVD, STB,...)

Functions

Analog to Digital Converters (A/D, D/A): MMI functions, battery & converters, temperature monitoring, control systems
Bus Controller: Telecom, consumer electronics, automotive, Hi-Fi systems, PCs, servers
Bus Repeater, Hub & Expander: Telecom, consumer electronics, automotive, Hi-Fi systems, PCs, servers
Real Time Clock (RTC)/Calander: Telecom, EDP, consumer electronics, clocks, automotive, Hi-Fi systems, FAX, PCs, terminals
DIP Switch: Telecom, automotive, servers, battery & converters, control systems
LCD/LED Display Drivers: Telecom, automotive instrument driver clusters, metering systems, POS terminals, portable items, consumer electronics
General Purpose Input/Output (GPIO) Expanders and LED Display Control: Servers, keyboard interface, expanders, mouse track balls, remote transducers, LED drive, interrupt output, drive relays, switch input
Multiplexer & Switch: Telecom, automotive instrument driver clusters, metering systems, POS terminals, portable items, consumer electronics
Serial RAM/ EEPROM: Scratch pad/ parameter storage
Temperature & Voltage Monitor: Telecom, metering systems, portable items, PC, servers
Voltage Level Translator: Telecom, servers, PC, portable items, consumer electronics

Semiconductors





Analog to digital converter

These devices translate between digital information communicated via the I²C bus and analog information measured by a voltage.

Analog to digital conversion is used for measurement of the size of a physical quantity (temperature, pressure …), proportional control or transformation of physical amplitudes into numerical values for calculation.

Digital to analog conversion is used for creation of particular control voltages to control DC motors or LCD contrast.

Bus controller

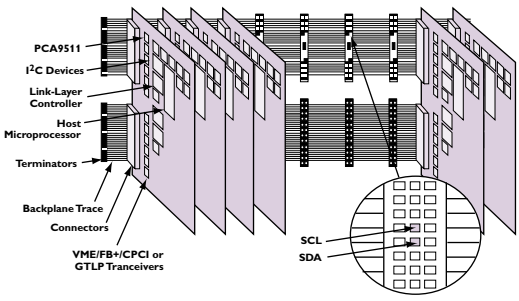
The master can be either a bus controller or µcontroller and provides the brain behind the I²C bus operation. A bus controller adds I²C bus capability to a regular µcontroller without I²C, or adds more I²C ports to µcontrollers already equipped with an I²C port such as the:

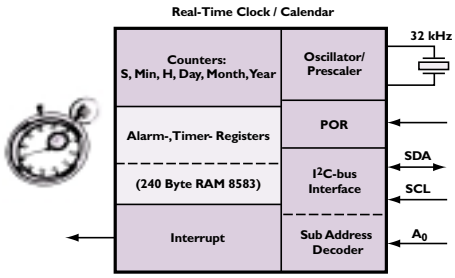
- P87LPC76x— > 100 kHz I²C
- P89C66x/65x/55x— > 100 kHz I²C
- P89LPC932— > 400 kHz I²C

Microcontrollers with multiple serial ports can convert from

- I²C to UART/RS232—LPC76x, 89C66x and 89LPC9xx
- I²C to SPI—P87C51MX and 89LPC9xx family
- I²C to CAN—8 bit P87C591 and 16 bit PXA-C37

General Purpose Device	Description	Features																									
		# of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit/total mA)	Internal Pull Up Current Source/Resistor on I/O	Vcc RANGE (V)						FREQ (kHz)			TEMP (°C)			Packages								
							1.0	1.8	2.5	3.3	5	5V TOLERANT	100	400	3400	0 to 70	- 40 to 85	- 55 to 125	PIN COUNT	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN
Analog / Digital Converter																											
PCF8591	4 ch A/D and 1 ch D/A with 8-bit accuracy	8							●	●	●	●	●				●		16	P		T				
Bus Controller																											
PCA9564	8051 based	128	0-1	●					●	●		●	●	●			●		20			D			PW	BS
PCF8584	80XX and Motorola 68000 based with snoop and long distance modes	128	0-1	●							●	●	●				●		20	P		T				





Bus repeater, hub & expander

Repeaters, hubs or expanders isolate the I²C bus loading into multiple 400 pF segments, the maximum limit imposed by the I²C specification for proper bus operation, by regenerating the I²C clock and data signals allowing many more devices than previously possible to communicate across the same bus. Hot swapping of cards into an active system is also now possible in addition to allowing mixed systems of both newer 3.3 V and older 5 V devices, opto-isolation of power supplies/medical systems, multi-point node connections, long distance wire transmission and RF links.

Clock & calendar

Real time clocks and event counters count the passage of time and act as a chronometer. They are used in applications such as periodic alarms for safety applications, system energy conservation, time and date stamp for point of sales terminals or bank machines.

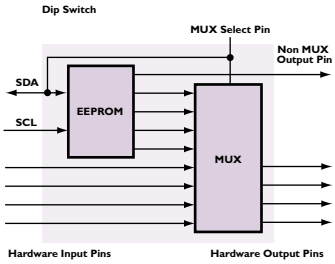
General Purpose Device	Description	Features																										
		# of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit/total mA)	Internal Pull Up Current Source/Resistor on I/O	Vcc RANGE (V)						FREQ (kHz)			TEMP (°C)			Packages								
							1.0	1.8	2.5	3.3	5	5V TOLERANT	100	400	3400	0 to 70	- 40 to 85	- 55 to 125	PIN COUNT	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN
Bus Repeater, Hub & Expander																												
P82B715	Long distance and multi-point	NA								●	●	●	●				●		8	PN	TD				DP	
P82B96	Long distance, multi-point, opto-isolation and level shifting	NA							●	●	●	●	●	●			●		8	PN	TD				DP	
PCA9511/13/14	Backplane buffer with idle detect, rise time accelerator, precharge	NA								●	●	●	●	●			●		8		D				DP	
PCA9512	Backplane buffer with idle detect, rise time accelerator, precharge, split V_{CC}s	NA								3.3 & 5.5		●	●	●			●		8		D				DP	
PCA9515	Repeater with 2 segments of 400 pF	NA								●		●	●	●			●		8		D				DP	
PCA9516	Hub with 5 segments of 400 pF	NA								●		●	●	●			●		16		D				PW	
PCA9518	Expandable Hub with 5 segments of 400 pF	NA								●		●	●	●			●		20			D			PW	
Clock & Calendar																												
PCF8563	Real Time Clock/Calendar with low voltage monitor	1	0-1				●	●	●	●	●	●	●	●			●		8	PN		TD			DP	
PCA8565	Expanded temperature range of PCF8563	1	0-1				●	●	●	●	●	●	●	●		-40 to 125			8	PN		TD			DP	
PCF8573	Real Time Clock/Calendar with low voltage monitor	4					1.1	●	●	●	●	●	●				●		16	PN		TD				
PCF8583	Real Time Clock with 240 bytes of scratch pad RAM	2	0-1				●	●	●	●	●	●	●				●		8	PN	TD					
PCF8593	Low Power Real Time Clock/Calendar	1	0-1	●			●	●	●	●	●	●	●				●		8	N		TD				

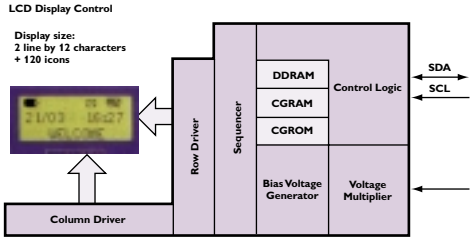
DIP switch

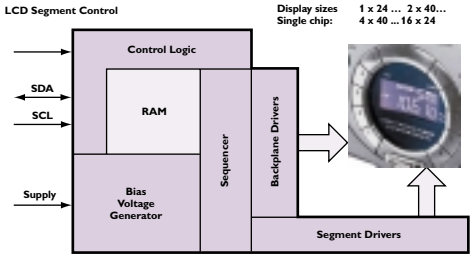
These devices serve as replacements for jumpers or dip switches and eliminate the need to open the equipment cabinet to modify settings manually, making it easier and less likely to damage the equipment. I²C commands and/or hardware pins are used to select between the default values or the setting programmed from the I²C bus and stored in the onboard I²C EEPROM register. The non-volatile I²C EEPROM register values stay resident even when the device is powered down and the devices power up with these values on the hardware output pins.

Display drivers

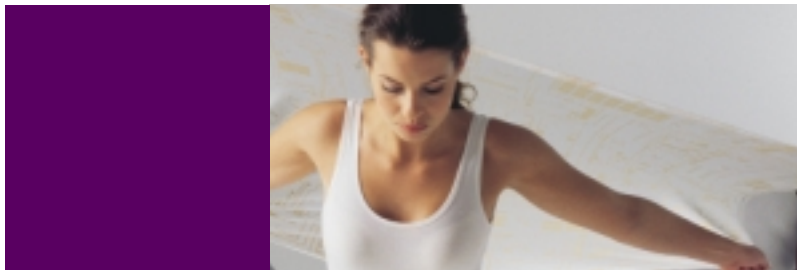
LCD display control provide the power to segments of an LCD that are controlled via the I²C bus. The LCD display control is an example of how "complete" a system an I²C device can be (e.g. generates the LCD voltages, adjusts the contrast, temperature compensates, stores the messages, has CGROM and RAM, etc.) The segment LCD control is a less complex LCD driver (e.g., just a segment driver).

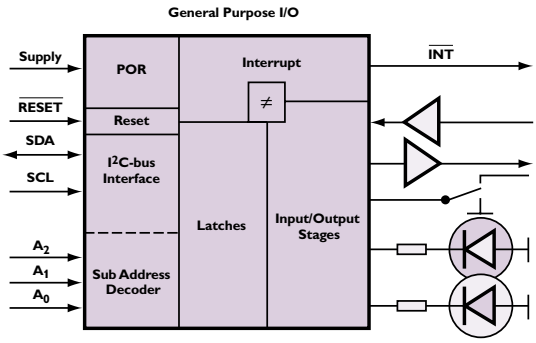






General Purpose Device	Description	# of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit/total mA)	Internal Pull Up Current Source/Resistor on I/O	Vcc RANGE (V) 1.0	1.8	2.5	3.3	5	5V TOLERANT	FREQ (kHz) 100	400	3400	TEMP (°C) 0 to 70	- 40 to 85	- 55 to 125	Packages PIN COUNT	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN
DIP Switch																										
PCA8550	4 input, 5 output with 1 EEPROM register	1								●		●	●	●		●			16		D		DB		PW	
PCA9559	5 input, 6 output with 1 EEPROM register	4			20-80					●		●	●	●		●			20						PW	
PCA9560	5 input, 6 output with 2 EEPROM register	4			25-100					●		●	●	●		●			20			D			PW	
PCA9561	5 input, 6 output with 4 EEPROM register	4			25-100					●		●	●	●		●			20			D			PW	
Display Drivers																										
	LCD Segment Driver																									
PCF8533	320 segment	16						●	●	●	●	●	●	●			●			Bare Die						
PCF8566	96 segment	16							●	●	●	●	●				●		40	Bare Die & VSO40						
OM4085	96 segment	16						2	●	●	●	●	●				●		40	Bare Die & VSO40						
PCF8576C	160 segment	16							●	●	●	●	●				●		56/64	Bare Die & VSO56/LQFP64						
PCF8576D	160 segment	16							●	●	●	●	●				●		56/64	Bare Die & TQFP64						
PCF8577C	64 segment	16							●	●	●	●	●				●		40	Bare Die & VSO40						
PCF8578	384+ segment	2							●	●	●	●	●				●		56/64	Bare Die & VSO56/LQFP64						
PCF8579	extension for PCF8578	2							●	●	●	●	●				●		56/64	Bare Die & VSO56/LQFP64						
	LCD Character Driver																									
PCF2103	24 character	2						●	●	●	●	●	●	●			●			Bare Die						
PCF2104	48 character	2							●	●	●	●	●				●			Bare Die						
PCF2105	48 character	2							●	●	●	●	●	●			●			Bare Die						
PCF2113	24 character + 120 icon	2						●	●	●	●	●	●	●			●		100	Bare Die & LQFP100						
PCF2116	48 character	2							●	●	●	●	●				●			Bare Die						
PCF2119	32 character	2		●					●	●	●	●	●	●			●			Bare Die						
	LCD Graphic Black/White Driver																									
PCF8531	34 x 128	2		●				●	●		●	●	●	●			●			Bare Die						
PCF8535	(65 + icon row) x 133	4		●							●	●	●	●			●			Bare Die						
PCF8548	65 x 102	2		●					●	●	●	●	●	●			●			Bare Die						
PCF8811	80 x 128	4		●			1.5	●	●	●	●	●	●	●	●		●			Bare Die						
PCF8813	(67 + icon row) x 102	4		●				●	●	●	●	●	●	●	●		●			Bare Die						
PCF8814	80 x 96	4		●				●	●	●		●	●	●	●		●			Bare Die						
	LCD Graphic Grey Scale Driver																									
PCF8820	67 x 101 4 grayscale	4		●					●	●	●	●	●	●			●			Bare Die						
PCF8821	33 x 101 4 grayscale	4		●					●	●	●	●	●	●			●			Bare Die						
OM6208	65 x 96 4 grayscale	16							●	●	●	●	●	●	●		●			Bare Die						
	LCD Graphic Color STN																									
PCF8831/32	160 x 128 RGB 256 color	4		●			1.5	●	●	●		●	●	●	●		●			Bare Die						
PCF8833	132 x 132 RGB 4 k color	4		●			1.7	●	●	●		●	●	●	●		●			Bare Die						
PCF8835	68 x 98 RGB 4 k color	4		●			1.7	●	●	●		●	●	●	●		●			Bare Die						



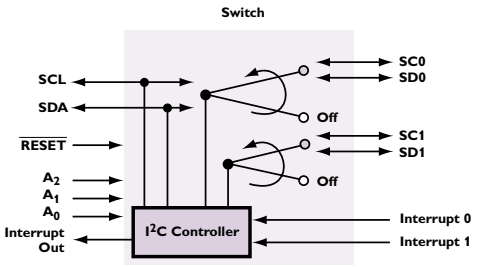


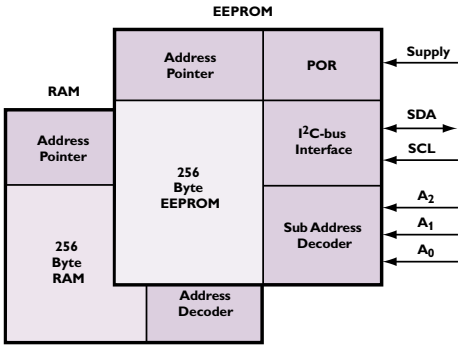
General purpose I/O and LED display control

General Purpose Digital input/output (GPIO) monitor 'YES' or 'NO' information, such as whether or not a switch is closed or a tank overflows. They can also be used to control a contact, turn on or off an LED, turn off a relay, start or stop a motor, or read a digital number presented at the port (via a DIP switch, for example). The I/Os are either open drain I/Os with a weak pull-up current source/resistor or totem pole outputs.

LED display control devices provide power to digital segments or LEDs that are controlled via the I²C bus. The new LED blinkers and dimmers have an internal oscillator and two internal PWMs that can be set to blink LEDs between 160 Hz and 6.3 seconds. This frees up a timer on the bus master and reduces the amount of bus traffic.

General Purpose Device	Description	Features																										
		# of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit/total mA)	Internal Pull Up Current Source/Resistor on I/O	Vcc RANGE (V)						FREQ (kHz)			TEMP (°C)			Packages									
							1.0	1.8	2.5	3.3	5	5V TOLERANT	100	400	3400	0 to 70	- 40 to 85	- 55 to 125	PIN COUNT	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN			
General Purpose I/O and LED Display Control																												
	Open Drain Outputs																											
PCA9500	8 bit with 2 kbit EEPROM	2-8			25-100	●				●		●	●	●			●		16			D			PW	BS		
PCA9501	8 bit with 2 kbit EEPROM and 6 address pins	2-64	0-1		25-100	●				●		●	●	●			●		20			D			PW	BS		
PCA9530	2 bit with 2 PWM - 160 Hz to 1.6 sec	2		●	25-50				●	●	●	●	●	●			●		8		D				DP			
PCA9531	8 bit with 2 PWM - 160 Hz to 1.6 sec	8		●	25-100				●	●	●	●	●	●			●		16		D				PW	BS		
PCA9532	16 bit with 2 PWM - 160 Hz to 1.6 sec	8		●	25-200				●	●	●	●	●	●			●		24			D			PW	BS		
PCA9533	4 bit with 2 PWM - 160 Hz to 1.6 sec	2			25-100				●	●	●	●	●	●			●		8		D				DP			
PCA9550	2 bit with 2 PWM - 40 Hz to 6.4 sec	2		●	25-50				●	●	●	●	●	●			●		8		D				DP			
PCA9551	8 bit with 2 PWM - 40 Hz to 6.4 sec	8		●	25-100				●	●	●	●	●	●			●		16		D				PW	BS		
PCA9552	16 bit with 2 PWM - 40 Hz to 6.4 sec	8		●	25-200				●	●	●	●	●	●			●		24			D			PW	BS		
PCA9553	4 bit with 2 PWM - 40 Hz to 6.4 sec	2			25-100				●	●	●	●	●	●			●		8		D				DP			
PCA9558	8 bit with 2 kbit EEPROM and 5 input, 6 output with 1 EEPROM register DIP Switch	2			25-100					●		●	●	●		●			28						PW			
PCF8574/74A	8 bit - A is alternate I²C address version	4	0-1		20-100	●			●	●	●	●	●				●		16	P		T	TS20						
PCF8575	16 bit	8	0-1		20-100	●			●	●	●	●	●	●			●		24				TS						
PCF8575C	Low Power version of PCF8575	8	0-1		20-100				●	●	●	●	●	●			●		24				TS						
SAA1064	4 x 8 Segment LED Controller	4			21						●	●	●				●		24	P	T								
	Totem Pole (Push-Pull) Outputs																											
PCA9534	Low Power version of PCA9554	8	0-1		25-100				●	●	●	●	●	●			●		16			D	DB		PW	BS		
PCA9535	Low Power version of PCA9555	8	0-1		25-200				●	●	●	●	●	●			●		24			D	DB		PW	BS		
PCA9554/54A	8 bit - A is alternate I²C address version	8	0-1		25-100	●			●	●	●	●	●	●			●		16			D	DB		PW	BS		
PCA9555	16 bit	8	0-1		25-200	●			●	●	●	●	●	●			●		24			D	DB		PW	BS		
PCA9556	8 bit	8		●	20-80					●	●		●			●			16						PW			
PCA9557	Improved version of PCA9556	8		●	25-100				●	●	●	●	●	●			●		16		D				PW	BS		





Multiplexer & Switch

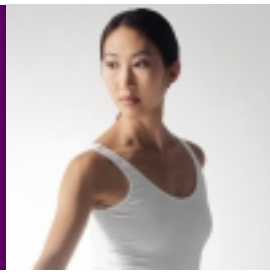
The multiplexers or switch fan one SCL/SDA channel to multiple downstream SCx/SDx channels that are selected by I²C commands. The multiplexers can select only one downstream SCx/SDx channel at a time whereas the switches can select multiple downstream SCx/SDx channels at a time making them useful as multiplexers in addition to voltage translators. Used in video projectors, servers or any other application where there is an address conflict (e.g., SPD EEPROMs on DIMMs), a need to isolate I²C sub-branches to reduce capacitive loading or to provide I²C bus voltage level shifting.

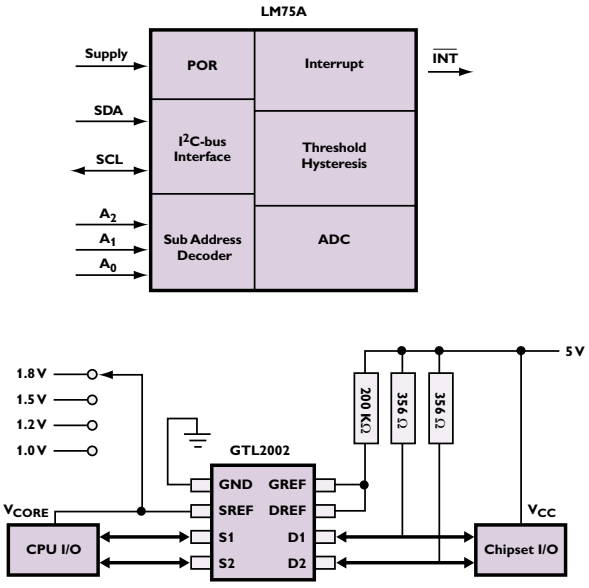
Serial EEPROM & RAM

RAM: Random Access Memory
EEPROM: Electrically Erasable Programmable Read On Memory

Common small serial memories are used in multiple applications. EEPROMs are particularly useful in applications where data retention during power-off is essential (for example: meter readings, electronic key, product identification number, etc). EEPROMs store data (2 kbits organized in 256 X 8 in the PCF8582C-2 for example), including your set points, temperature, alarms, and more, for a guaranteed minimum storage time of ten years in the absence of power. EEPROMs are capable of being programmed 1,000,000 times and have an infinite number of read cycles.

General Purpose Device	Description	Features																								
		# of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit/total mA)	Internal Pull Up Current Source/Resistor on I/O	Vcc RANGE (V)						FREQ (kHz)			TEMP (°C)			Packages							
							1.0	1.8	2.5	3.3	5	5V TOLERANT	100	400	3400	0 to 70	- 40 to 85	- 55 to 125	PIN COUNT	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN
Multiplexer & Switch																										
PCA9540	1 to 2 Multiplexer	1							●	●	●	●	●	●			●		8		D				DP	
PCA9541	2 to 1 Demultiplexer with Interrupt	16	1-2	●					●	●	●	●	●	●			●		16		D				PW	BS
PCA9542	1 to 2 Multiplexer with Interrupt	8	2-1						●	●	●	●	●	●			●		14		D				PW	
PCA9543	1 to 2 Switch with Interrupt	4	2-1	●					●	●	●	●	●	●			●		14		D				PW	
PCA9544	1 to 4 Multiplexer with Interrupt	8	4-1						●	●	●	●	●	●			●		20			D			PW	BS
PCA9545	1 to 4 Switch with Interrupt	4	4-1	●					●	●	●	●	●	●			●		20			D			PW	BS
PCA9546	1 to 4 Switch	8		●					●	●	●	●	●	●			●		16		D				PW	BS
PCA9548	1 to 8 Switch	8		●					●	●	●	●	●	●			●		24			D			PW	BS
Serial EEPROM & RAM																										
PCA8581(C)	1 Kbit EEPROM	8							C	C	●	●	●			-25 to 85			8	N	D					
PCF85102C-2	2 Kbit EEPROM	8							●	●	●	●	●				●		8	N	D					
PCF85103C-2	2 Kbit EEPROM with alternate I²C address	8							●	●	●	●	●				●		8	N	D					
PCF85116-3	16 Kbit EEPROM	1								●	●	●	●	●			●		8	N	D					
PCF8570	2 Kbit RAM	8							●	●	●	●	●				●		8	P	T					
PCF8582C-2	2 Kbit EEPROM	8							●	●	●	●	●				●		8	N	D					
PCF8594C-2	4 Kbit EEPROM	4							●	●	●	●	●				●		8	N	D					
PCF8598C-2	8 Kbit EEPROM	2							●	●	●	●	●				●		8	N		D				





Temperature & voltage monitor

Hardware Monitors sense the system temperature and/or voltage and use the I^2C bus to report the temperature and/or voltage. Some of the temperature monitors include hardware pins that allow transistors/diodes to be located in external components (e.g., processors) so that the temperature is sensed much more accurately than if the sensor was mounted externally on the package.

Voltage level translator

The voltage level translators provide bi-directional level translation without the need for a direction control pin, to and from any voltage between 1.0 V and 5.0 V. They are open drain on both sides of the device, with no drive (no V_{CC}). The reference voltage clamps the output voltage, allowing the voltage translation with a very low propagation delay. BiCMOS processing provides excellent ESD performance. A typical application for these devices is the translation of a lower voltage ASIC I^2C port to a higher voltage 3.3 V and/or 5.0 V I^2C bus/chipset.

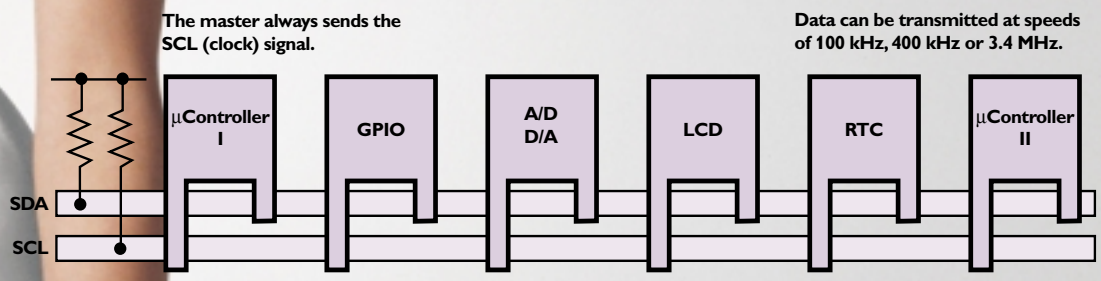
General Purpose Device	Description	Features																								
		# of Addresses	Interrupt (In/Out)	Hardware Reset	Current (per bit/total mA)	Internal Pull Up Current Source/Resistor on I/O	Vcc RANGE (V)						FREQ (kHz)			TEMP (°C)			Packages							
							1.0	1.8	2.5	3.3	5	5V TOLERANT	100	400	3400	0 to 70	- 40 to 85	- 55 to 125	PIN COUNT	DIP	SO (narrow)	SO (wide)	SSOP	QSOP	TSSOP	HVQFN
Temperature and Voltage Monitor																										
LM75A	Temperature Sensor and Thermal WatchDog with resolution of 0.125°C and accuracy of +/- 2°C	8	0-1						2.8	●	●		●	●				●	8		D				DP	
NE1617A	Temperature Sensor with accuracy of +/- 2°C on chip and +/- 3°C remote sensor	9								●	●	●	●			0 to 125			16					DS		
NE1618	High Accuracy Temperature Sensor with accuracy of +/- 2°C on chip and +/- 1.5°C w/1.0°C resolution or +/- 1.0°C w/0.125 C resolution on remote sensor	9								●		●	●			0 to 125			16					DS		
NE1619	HECETA 4 Temperature and Voltage Monitor—resolution of 1°C and accuracy of +/- 2°C on chip and +/- 3°C remote sensor and monitor 12 V, 5 V, 3.3 V, 2.5 V, V_{CCP}, V_{DD}	2								●	●	●	●	●		0 to 125			16					DS		
Voltage Level Translators																										
GTL2000	22 bit - 1.0 V through 5.0 V Translator						●	●	●	●	●	●	●	●			●		48				DL		DGG	
GTL2002	2 bit - 1.0 V through 5.0 V Translator						●	●	●	●	●	●	●	●			●		8						DP	
GTL2010	10 bit - 1.0 V through 5.0 V Translator						●	●	●	●	●	●	●	●			●		8						PW	BS

How I^2C works

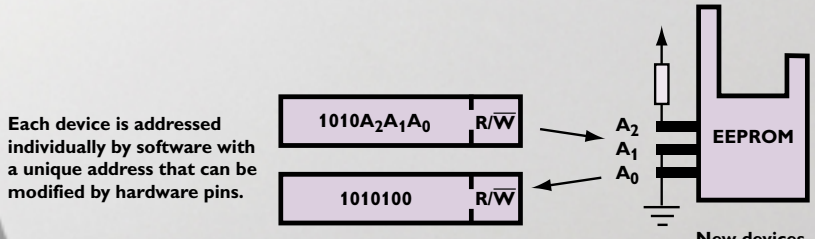
Any I^2C device can be attached to a common I^2C bus and every device can talk with any master, passing information back and forth. The I^2C bus (or its derivatives such as SMBus, DDB, etc) is the only 2-wire bus where devices are addressed completely by software.

Each device must have a unique 7-bit I^2C address so that the master knows specifically who it is communicating with. Typically the first four bits are fixed and assigned to specific categories of devices, e.g. 1010 is assigned to serial EEPROMs. The next three bits (e.g., A_2, A_1 and A_0) are set by hardware address pins on the package that modify the I^2C address allowing up to eight different address combinations and therefore allowing up to eight identical devices to operate on the I^2C bus. These pins are held high to V_{CC} (1) or held low to GND (0).

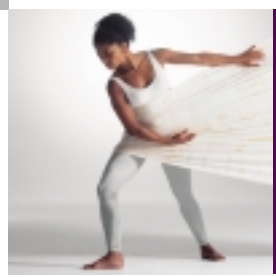
The last bit of the initial byte indicates if the master is going to send (write) or receive (read) data from the receiver, typically a slave device. Each transmission sequence must begin with the start condition and end with the stop or restart condition. If there are two masters on the same bus, there are arbitration procedures if both try to take control of the bus at the same time. Once a master (e.g., microcontroller) has control, no other master can take control until the first master sends a stop condition and places the bus in an idle state.



The open drain/collector outputs provide for a "wired-AND" connection that allows devices to be added or removed without impact and always requires a pull-up resistor.



New devices or functions can be easily clipped on to an existing bus!



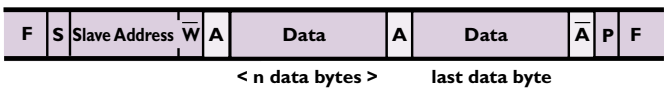
I²C bus terminology

- Transmitter—the device that sends data to the bus. A transmitter can either be a device which puts data on the bus of its own accord (a 'master-transmitter'), or in response to a request from data from another device (a 'slave-transmitter').
- Receiver—the device that receives data from the bus.
- Master—the component that initiates a transfer, generates the clock signal and terminates the transfer. A master can be either a transmitter or a receiver.
- Slave—the device addressed by the master. A slave can be either receiver or transmitter.
- Multi-master—the ability for more than one master to co-exist on the bus at the same time without collision or data loss.
- Arbitration—the prearranged procedure that authorizes only one master to take control of the bus at a time.
- Synchronization—the prearranged procedure that synchronizes the clock signals provided by two or more masters.
- SDA—data signal line (Serial DAta)
- SCL—clock signal line (Serial CLock)

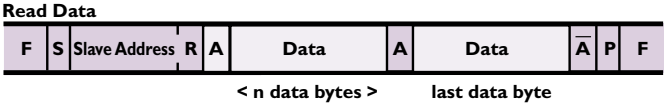
Terminology for bus transfer

- F (FREE)—the bus is free or idle; the data line SDA and the SCL clock are both in the high state.
- S (START) or S_R (Repeated START)—data transfer begins with a start condition. The level of the SDA data line changes from high to low, while the SCL clock line remains high. When this occurs, the bus becomes 'busy'.
- C (CHANGE)—while the SCL clock line is low, the data bit to be transferred can be applied to the SDA data line by a transmitter. During this time, SDA may change its state as long as the SCL line remains low.
- D (DATA)—a high or low bit of information on the SDA data line is valid during the high level of the SCL clock line. This level must be kept stable during the entire time that the clock remains high, to avoid misinterpretation as a Start or Stop condition.
- P (STOP)—data transfer is terminated by a stop condition. This occurs when the level on the SDA data line passes from the low state to the high state, while the SCL clock line remains high. When the data transfer has been terminated, the bus becomes free once again.

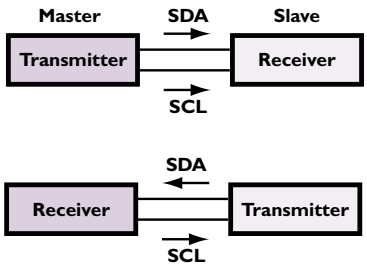
Write Data



Read Data



S = Start condition **A = Acknowledge**
F = Free **R/$\overline{W}$ = read / Not write**
P = Stop condition **$\overline{A}$ = Not Acknowledge**



Philips Semiconductors

Philips Semiconductors is a worldwide company with over 100 sales offices in more than 50 countries. For a complete up-to-date list of our sales offices please e-mail
sales.addresses@www.semiconductors.philips.com.
A complete list will be sent to you automatically.
You can also visit our website
http://www.semiconductors.philips.com/sales.

www.semiconductors.philips.com

date of release: December 2002
document order number: 9397 750 10591

Printed in U.S.A.

www.semiconductors.philips.com/logic/i2c

Purchase of Philips I²C components conveys a license under the Philips' patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips.